

Product-sum photonic integrated circuit based on microring resonators and MMI coupler on SOI

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Abstract—A product-sum photonic integrated circuit consisting of SOI-based cascaded microring modulators and a 4×1 multimode interference coupler is proposed for CNN computing. A basic product-sum operation is numerically demonstrated for 2×2 matrix.

Keywords—microring modulator, optical signal processing

I. INTRODUCTION

It is hard for conventional electrical integrated circuits to satisfy the exponentially increasing bandwidth requirements for computing systems due to their intrinsic speed limitation. Silicon photonics has therefore attracted much academic and industrial attention due to its use of the advantages of light, such as low propagation loss, low latency, large bandwidth and low power consumption, as well as its compatibility with complementary metal-oxide-semiconductor (CMOS) fabrication processes [1]. For optical computing and signal processing, a unique circuit architecture called “Direct Logic” has been proposed [2]. This architecture utilizes the strengths of both optics and electronics, and various optical logic gates and circuits based on directed logic, such as AND/NAND, OR/NOR gates [3], XOR/XNOR gates [4], half adders [5], and full adders [6], have been reported. A convolutional neural network (CNN) has become a representative algorithm of deep learning, demonstrating high performance in computer vision tasks such as image classification, object detection and object localization. Utilizing a CNN in the optical domain instead of a conventional electrical circuit can provide benefits, such as high-speed calculation and low latency. However, few optical circuits for CNN computing have been reported.

In this paper, a new photonic circuit computing the sum of products for a CNN is proposed. This circuit utilizes direct-logic-based AND gates composed of two microring modulators (MRMs) [3] to be designed as a photonic integrated circuit based on the silicon-on-insulator (SOI). The basic product-sum operation of the circuit is evaluated for a 2×2 matrix at 1.0 Gbit/s via simulation.

II. CIRCUIT DESIGN

Fig. 1(a) presents a simple example of convolution computing in image processing. A filter matrix is set for extracting a feature from an input image and applied to a window in the image. The filter and window have the same matrix size, and the sum of their dot products (S) is computed as follows:

$$S = A_1Q_1 + A_2Q_2 + A_3Q_3 + A_4Q_4$$

Here, A_m ($m = 1, 2, 3, 4$) is an element of the window in the input image, and Q_m ($m = 1, 2, 3, 4$) is an element of the filter. The filter scans the input image two-dimensionally and product-sums are computed at every spatial position. Then, a convolved feature is finally obtained.

For convolving an input matrix with a 2×2 filter, a photonic computing circuit for the product-sum operation is proposed. As illustrated in Fig. 1(b), the circuit comprises four sets of cascaded MRMs, a 4×1 multimode interference (MMI) coupler and a single-mode light source. Input signals A_m and Q_m ($m = 1, 2, 3, 4$) are elements of the 2×2 matrices. A_m and Q_m are electrical binary (0 or 1) signals that are applied to the first and second MRMs, respectively, after being converted to the driving voltage signals. Each of two MRMs modulates the continuous wave (CW) light from the light source and an optical output, P_m , from the cascaded MRMs corresponding to a product (or logic AND) of A_m and Q_m . Only when both A_m and Q_m are “1” (ON state) can the CW light path through two MRMs, and P_m becomes “1”. Four optical output signals (P_m , $m = 1, 2, 3, 4$) are combined through the 4×1 MMI coupler and are output as S , which indicates the product-summation of the 2×2 window and 2×2 filter.

III. DESIGN OF COMPONENT

The proposed circuit was designed for a photonic integrated circuit based on the SOI optical waveguide. Fig. 2 presents the cross-sectional diagram of waveguides models in the MRM. As illustrated in Fig. 2(a), a Si core with a height of 220 nm and width of 450 nm is set on a SiO_2 under clad layer and the core is covered with SiO_2 over clad. The ring waveguide incorporates a p-n junction, as shown in Fig. 2(b),

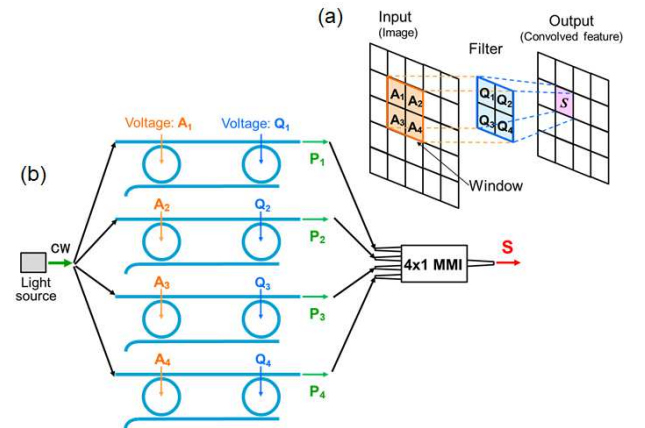


Fig. 1 (a) Schematic of image convolution. (b) Diagram of photonic computing circuit for product-sum operation.

for modulation. The ring radius and ring-bus gap shown in

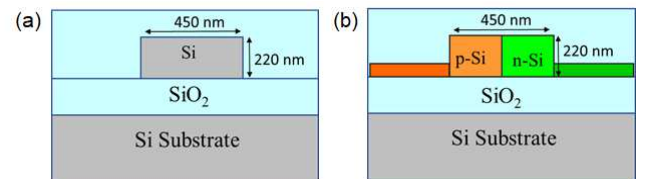


Fig. 2 Cross section of SOI waveguide models; (a) Passive waveguide. (b) P-N junction region in the microring.

Fig. 3(a) are set to $5.0\ \mu\text{m}$ and $0.15\ \mu\text{m}$, respectively. The MRM operates at depletion-mode [7] and its calculated transmission spectra at different bias voltages are shown in Fig. 3(b). The Q-factor and static modulation efficiency of the MRM are about 5000 and 60 pm/V, respectively. Considering the trade-off between the insertion loss and extinction ratio of the MRM, the operating wavelength is set to 1539.44 nm. When the driving voltage is set to $1.5\ \text{V}_{\text{p-p}}$ ($-1.5 \sim 0.0\ \text{V}$), an insertion loss of 6.0 dB and an extinction ratio of 8.6 dB are expected.

The 4×1 MMI coupler was also designed on the same SOI. It has multimode waveguide with a length of $5.1\ \mu\text{m}$ and width of $3.5\ \mu\text{m}$, and tapered waveguide design is applied to five ports. All four input ports have almost the same transfer parameters to the output port. The calculated total insertion loss of the MMI coupler is 6.2 dB.

IV. DYNAMIC OPERATION OF CIRCUIT

To verify the basic operation of the photonic computing circuit, the circuit operation is simulated with 1-Gbit/s input electrical signals, A_m and Q_m . The logic 0 and 1 are input to the MRMs as bias voltages of -1.5 and $0.0\ \text{V}$, respectively. Fig. 4(a) and (b) present A_I and Q_I signals, respectively, with

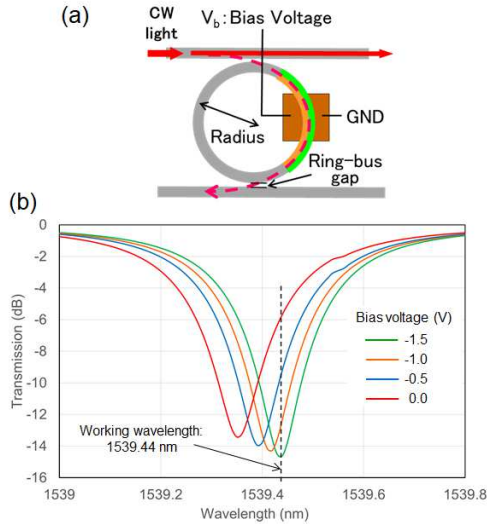


Fig. 3 (a) Schematic diagram of microring modulator. (b) Calculated transmission spectra of microring modulator.

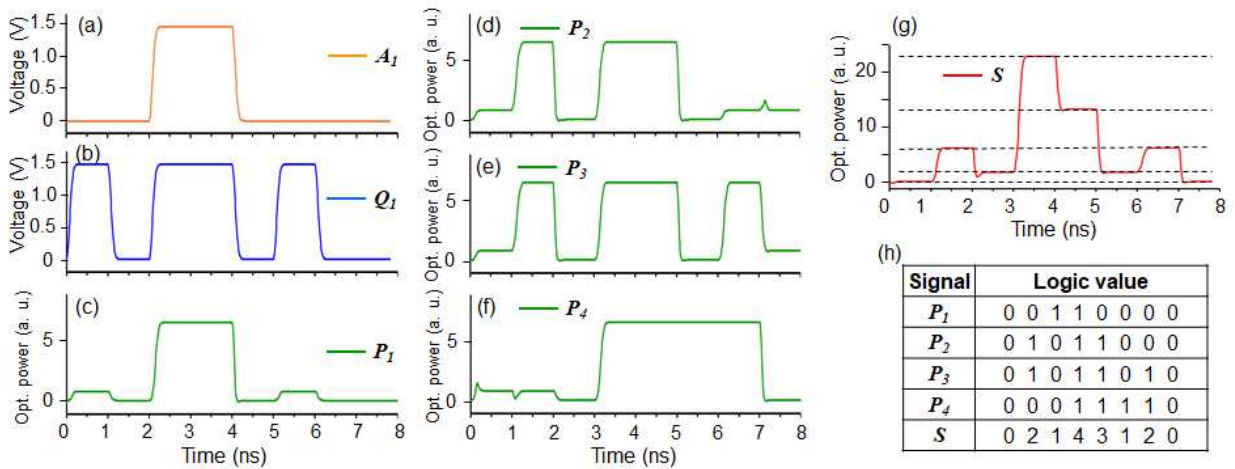


Fig. 4. Simulated product-sum operation at 1 Gbit/s. (a) A_I : Input to the first MRM; (b) Q_I : Input to the second MRM; (c) P_I : Output of the cascaded MRMs; (d) P_2 ; (e) P_3 ; (f) P_4 ; (g) S : Output of MMI coupler; (h) logic values.

rectangular wave shapes. Ideal single-mode light with a wavelength of 1539.44 nm is input into the cascaded MRMs, and is modulated and observed as optical output P_I , as shown in Fig. 4(c). P_I correctly indicates the product of A_I and Q_I . Similarly, P_2 , P_3 and P_4 , presented in Fig. 4(d), (e), and (f), respectively, correspond to the products of A_m and Q_m ($m = 2, 3, 4$), although not all input signals are provided in Fig. 4. P_1 , P_2 , P_3 and P_4 are combined by the 4×1 MMI coupler. The final output (S) is presented in Fig. 4(g). Five different power levels are clearly recognized as “0”, “1”, “2”, “3” and “4”, although the power levels are not in a linear relationship due to the intrinsic characteristics of the MMI coupler. As shown in Fig. 4(h), S properly indicates the sum of P_1 , P_2 , P_3 and P_4 . The total loss of the photonic circuit is estimated to be 18.2 dB, and can be reduced by adjusting the Q-factor of the MRMs and operating wavelength.

In conclusion, an SOI-based photonic circuit computing the sum of products for a CNN is proposed and demonstrated through simulation. The proposed circuit utilizes the direct-logic-based AND gate composed of cascaded MRMs to calculate the dot product of two binary input signals and the 4×1 MMI coupler to sum four products. The MRMs and MMI are designed for the $1.55\text{-}\mu\text{m}$ band and the basic product-sum operation of the circuit is verified for a 2×2 matrix. The proposed circuit serves as a preliminary step for future photonic CNN computing development.

REFERENCES

- [1] Richard A Soref, "Silicon-based optoelectronics," *Proceedings of the IEEE*, vol. 81, No. 12, pp. 1687-1706, 1993.
- [2] James Hardy and Joseph Shamir, "Optics inspired logic architecture," *Optics Express*, vol. 15, No. 1, pp 150-165, 2007.
- [3] Yonghui Tian *et al.*, "Proof of concept of directed OR/NOR and AND/NAND logic circuit consisting of two parallel microring resonators," *Optics Lett.*, vol. 36, No. 9, pp. 1650-1652, 2011.
- [4] Lei Zhang *et al.*, "Demonstration of directed XOR/XNOR logic gates using two cascaded microring resonators," *Optics Lett.*, vol. 35, No. 10, pp. 1620-1622, 2010.
- [5] Yonghui Tian *et al.*, "Directed optical half-adder based on two cascaded microring resonators," *IEEE Photon. Technol. Lett.*, vol. 24, No. 8, pp. 643-645, 2012.
- [6] Zhoufeng Ying *et al.*, "Silicon microdisk-based full adders for optical computing," *Optics Lett.*, vol. 43, No. 5, pp. 983-986, 2018.
- [7] M. Pantouvaki *et al.*, "Active Components for 50 Gb/s NRZ-OOK Optical Interconnects in a Silicon Photonics Platform," *IEEE J. Lightwave Technol.*, vol. 35, No. 4, pp. 631-638, 20