

Modeling of polarization-rotation based photonic D flip-flop using a compact micro-ring resonator

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Abstract— This paper demonstrates the modeling and simulation of all-optical polarization rotation based clocked D flip-flop using a single micro-ring resonator. The simulated results show the switching time of 0.5 ps and the on-off ratio of 25.27 dB.

Keywords- all-optical switch, FDTD simulation, micro-ring resonator, optical flip-flop, polarization rotation

I. INTRODUCTION

The flip-flops (FFs) are sequential logic circuits used for memory storage in digital form. The D-FF is a Delay FF having one-bit arithmetical memory. D-FF can be designed using the concept of electro-optic effect in the micro-ring resonator (MRR) [1] and Mach-Zehnder Interferometer [2]. In the present paper the implementation of D-FF is all-optical in nature with simple architecture [3-5], where polarization states are manipulated and the specific logic relationship has been obtained between the input and output signal. The output state of the polarized light is dependent on the nature of the polarization rather than its intensity.

II. THEORY AND OPERATION OF THE PROPOSED MODEL

The schematic of the proposed structure comprises of an MRR, a polarization-rotator (PR), and a feedback loop called an erbium-doped waveguide amplifier (EDWA) [6-7] is shown in Fig. 1. The PR is used to rotate the axis of unpolarized light to the polarized light by an angle of choice due to its birefringence effect. To realize the all-optical flip-flop switching, the EDWA is employed in the proposed design which is used to amplify the feedback signal and to provide the delay in the circuit [5]. The parameters used for modeling the device are given in Table I.

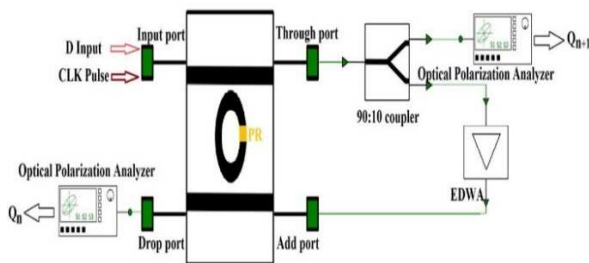


Fig. 1. Schematic diagram of the proposed model

TABLE I PARAMETERS USED FOR MODELLING

Parameters	Description
Material combination	Si-SiO ₂
Gain of EDWA	3 dB
Insertion loss	0.0002 dB
Circumference of the MRR	62.8 μ m
Coupling coefficient of MRR	TE = 0.2, TM = 0.15
Height of the waveguide	0.2 μ m
Width of the waveguide	0.4 μ m

III. RESULT AND DISCUSSIONS

In the D-FF, if the clock pulse is at “logic 1” or high, the output of D-FF (Q_{n+1}) is as same as D input and if the clock signal is at “logic 0” or low, the FF holds the data of the previous state. The input of the D-FF is active only when the control pulse is high. Thus, the D-FF is a controlled bi-stable latch.

For realizing the D-FF in the proposed device, “logic 1” or high is considered as horizontal polarized light (HPL), and “logic 0” or low is considered as vertical polarized light (VPL) respectively. The proposed MRR changes its output polarized state if the suitable nature of the pump pulse is injected. The corresponding transmission of the MRR and the electric field evolution in the proposed device are shown in Fig. 2 (a) and 2 (b) respectively.

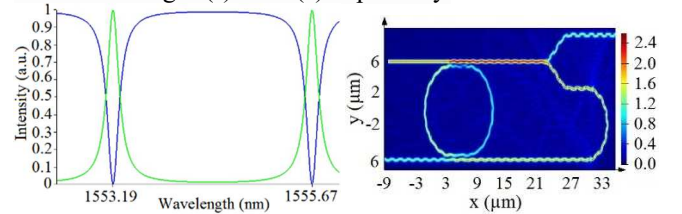


Fig. 2. (a). Output transmission of the MRR (b). Electric field evolution of the proposed model

To realize the FF, the D-input as well as the clock signal (CLK) are injected from the input port at resonance wavelengths (λ_r) of 1555.67 nm and 1553.19 nm respectively, through the coupler. At $\lambda_r = 1555.67$ nm, the polarization-rotation is realized at the outputs of the device through the optical polarization analyzer in terms of azimuth angle. The VPL has azimuth angle near to 90° and HPL has azimuth angle near to 0°. The output obtained from the through port via a Y-coupler (90:10 coupler) called the Q_{n+1} , and the rest part of the light is

amplified by the EDWA and feedback to MRR through the add port. The strong CLK pulse allows the output (Q_{n+1}) to alter its state; otherwise, it holds the former state. The PR has been fixed to provide a rotation of 30° . The various logical combinations for the proposed D-FF are as follows;

Case-1: $D = CLK = HPL$ ("logic 1"), $Q_n = HPL$ ("logic 1")

If the previous state (Q_n) is HPL, an optical pulse will reach at the add port passing through the feedback path. The signals are present at the input port and add port. When CLK is applied simultaneously, therefore, according to the principle of MRR, the D input is propagated towards the through port [5]. Consequently, the FF's next state (Q_{n+1}) is HPL. The graph in Fig. 3 (a) and Fig. 3 (b) shows the azimuth angle of 0° and less than 10° indicates the HPL at the output.

Case-2: $D = Q_n = HPL$ ("logic 1"), $CLK = VPL$ ("logic 0")

Similar to the previous case, the output signal arrives at add port after passing through the loop with the same instant of input D. Due to the low CLK pulse, the output nature of HPL is obtained at the through port, as shown in Fig. 3 (c). As the CLK signal is low (or VPL), therefore, according to the principle of MRR, the input optical signal is directed towards the drop port [5]. At the same instant, the signal of add port will be directed towards the through port of the MRR. The output is same as the previous state as shown in Fig. 3 (d).

Case-3: $D = VPL$ ("logic 0"), $CLK = Q_n = HPL$ ("logic 1")

When a strong CLK of HPL is injected into the device, the input D has been directed towards the through port. As a result, Q_{n+1} of VPL is observed at the output. The output of Q_{n+1} and Q_n is shown in Fig. 3 (e) and Fig. 3 (f) which indicates the azimuth angle of 80° and 10° and confirms the VPL and HPL respectively.

Case-4: $D = Q_n = CLK = VPL$ ("logic 0")

When the D-input is VPL as well as low CLK is applied to the device, the output of D-FF would be low, as shown in Fig. 3 (g) and Fig. 3 (h). The simulated results are summarized in Table II.

The performance of the device depends on the gain of the amplifier, the rotation angle of the PR, and the geometrical parameters of the device. The all-optical switching behaviour of the MRR is dependent on the circumference, which also determines resonance condition and thus, free-spectral range (FSR). The comparison of the proposed work with the recent literatures is shown in Table III.

TABLE II TRUTH-TABLE OF THE PROPOSED D-FF

D input	CLK	Q_{n+1}	Q_n	Remarks
"logic 1" HPL	"logic 1" HPL	"logic 1" HPL	"logic 1" HPL	Set
"logic 1" HPL	"logic 0" VPL	"logic 1" HPL	"logic 1" HPL	Unchanged
"logic 0" VPL	"logic 1" HPL	"logic 0" VPL	"logic 1" HPL	Reset
"logic 0" VPL	"logic 0" VPL	"logic 0" VPL	"logic 0" VPL	Unchanged

TABLE III COMPARISON WITH THE LITERATURES

References	Parameters			
	Circumference	FSR	On-off ratio	Response time
[1]	60 μm	-	-	0.04 ns
[5]	44.5 μm	-	21 dB	1.6 ps
This work	62.8 μm	2.5 nm	25.27 dB	0.5 ps ; 0.6 ps

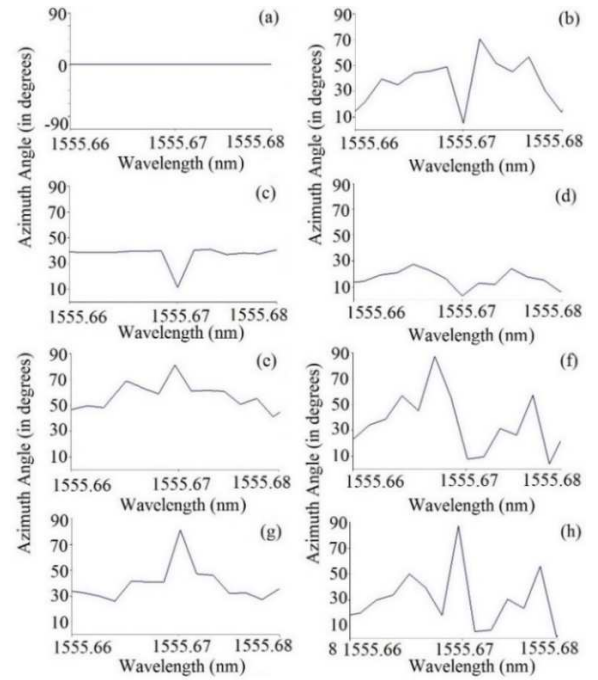


Fig. 3. (a)-(h). Outputs of the proposed model in terms of azimuth angle

IV. CONCLUSIONS

This paper demonstrates the polarization rotation based MRR for D-FF switching. The simulation results verified its successful operation. The model shows the on-off ratio of 25.27 dB and the response time of 0.5 ps. The FSR has been obtained as high as 2.5 nm. The model may be used for obtaining other sequential, combinational circuits and is suited for interconnects within micro or sub-microchips.

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