Solution-Processed Heterojunction Oxide Thin-Film Transistors for Displays

Wensi Cai
Key Laboratory of Optoelectronic Technology & Systems (Ministry of Education)
Chongqing University
Chongqing, China
wensi.cai@cqu.edu.cn

***Abstract*—In this study, we investigate the effect of channel layer thickness on the performance of InZnO/AlInZnO (IZO/AIZO) heterojunction thin-film transistors (TFTs) fabricated using a solution-based method. The conduction band offset at the heterointerface significantly influences the operating characteristics of TFTs, which can be modulated by adjusting the layer thickness, as confirmed through both experimental and computational analysis. Due to the formation of a quasi-two-dimensional electron gas system at the IZO/AIZO interface, optimized TFTs show a high mobility of ~18 cm^2/Vs, a near-zero turn-on voltage and a current on/off ratio approaching 10^8. The work offers valuable insights into the operating principles of oxide-based heterojunction TFTs and highlights their potential for next-generation printable displays.**

Keywords—oxide semiconductors, thin-film transistors, solution-processed, displays

I. Introduction

Amorphous oxide semiconductor based thin-film transistors (TFTs) fabricated by sputtering have been commercialized as backplane drivers for flat panel displays due to their superior electrical characteristics [1]. However, sputtering is not compatible with next-generation printable electronics. TFTs prepared by solution-based methods are thus desirable, but it is still quite challenging for them to achieve a mobility greater than 10 cm^2/Vs. In addition, residue organic species can lead to serious stability issues. As a result, solution-processed oxide TFTs reported to date still far short of the performance requirements for next-generation high-resolution displays.

Recently, we demonstrated that by adjusting the annealing temperature and/or doping the film with slight metal cations, the mobility and stability of solution-processed TFTs can be improved [2-5]. However, the mobility and current on/off ratio achieved so far remain insufficient. One promising approach to further improve device performance is to stack oxide semiconductors with different mobilities and carrier concentrations, as this can induce the formation of a quasi-two-dimensional electron gas (q2DEG) system at the heterointerface. However, such bilayer TFTs often suffer from various drawbacks, including negative turn-on and threshold voltages, and instability under negative bias illumination stress (NBIS). For displays, achieving stable operation under bias conditions and a near-zero turn-on voltage is essential.

In this work, we report IZO/AIZO heterojunction TFTs fabricated via a solution-based method. The influence of channel layer thickness on electron distribution and resulting device performance is systematically investigated. Through a combination of experimental measurements and simulations, we demonstrate optimized IZO/AIZO TFTs with a mobility of 17.6 cm^2/Vs and a good stability. The underlying mechanisms of thickness-dependent performance are thoroughly analyzed. This study provides useful insights for the further development of heterojunction transistor architectures and shows potential for applications in next-generation displays.

II. Experimental Procedures

A schematic of the prepared oxide TFT is shown in Fig. 1(a). The deposition process is similar to our previous work [6]. In this study, the AIZO layer (Al:In:Zn = 1:49.5:49.5 by volume) was fixed as 5.6 nm. Single channel IZO (In:Zn = 6:4 by volume) TFTs has a channel thickness of 7.2 nm. In the case of heterojunction TFTs, the IZO thickness was varied to 5, 7.2 and 10 nm, corresponding to devices labeled IZO-1/AIZO, IZO-2/AIZO and IZO-3/AIZO, respectively. Device simulations were performed using TCAD tools.

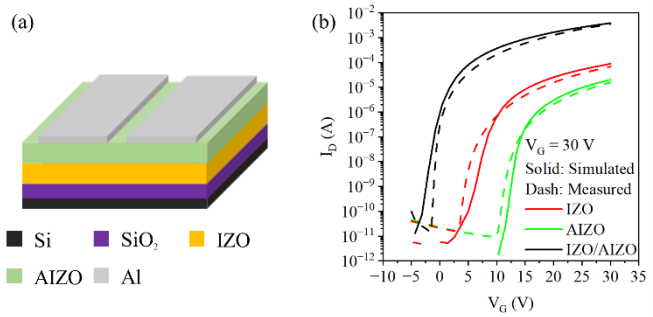

Fig. 1. (a) A schematic diagram showing the device structure. (b) Transfer characteristics of both simulated and measured device performance.

III. Results and Discussions

The transfer characteristics of IZO and AIZO TFTs are shown in Fig. 1(b), along with simulated transfer curves generated using TCAD based on the respective band structures of IZO and AIZO. In both devices, electrons are primarily located at the dielectric/channel interface, as expected, and the simulated characteristics closely match the experimental results.

The combination of IZO and AIZO in a heterojunction structure leads to a substantially enhanced mobility - from 0.2 (AIZO) and 0.6 (IZO) to 17.6 cm^2/Vs (IZO/AIZO). Additionally, the current on/off ratio is improved by approximately twofold, as shown in Fig. 1(b).

To investigate the conduction mechanism, TCAD simulations were carried out under both off- and on-states, as shown in Fig. 2. In the off and turn-on states, a potential well with a depth of ~300 meV forms near the IZO/AIZO heterointerface. However, under a large positive gate bias (on-state) the potential barrier is significantly reduced, and no potential well is observed. This suggests that free electrons

The work was financially supported by the National Natural Science Foundation of China (No. 62204027).

migrate from the heterointerface into the IZO channel near the IZO/SiO_2 interface. In single channel TFTs, electron accumulation occurs only at the channel/SiO_2 interface, while the heterojunction TFTs exhibit electrons accumulation at both the IZO/AIZO and the IZO/SiO_2 interface, indicating the formation of a quasi-2DEG system. This dual-interface electron accumulation enhances the total electron density in the channel and is considered the primary factor responsible for the enhanced device performance.

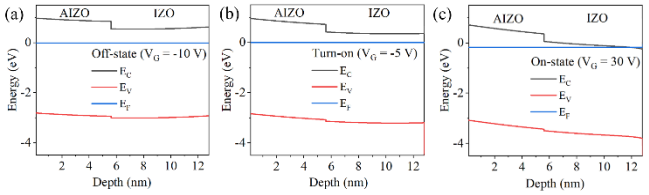

Fig. 2. TCAD simulation of band alignment in the (a) off-state, (b) turn-on state and (c) on-state.

To investigate the correlation between IZO thickness and the device performance, we conducted both TCAD simulations and experimental measurements, as shown in Fig. 3. A left shift of the transfer characteristics was observed with the increase of IZO thickness. This shift is attributed to the shift of CBM toward the Fermi level, leading to a greater energy band bending in thicker IZO cases and enhanced electron accumulation in the channel. However, excessive electron accumulation can make it difficult to turn off the TFT within the applied gate voltage range (IZO-3/AIZO), resulting in a reduced current on/off ratio. Additionally, the experimental data reveal that the mobility of IZO-3/AIZO TFT is slightly lower than that of the IZO-2/AIZO TFT. The reduction in mobility may be related to the limited Debye length, increased impurity scattering, or charge trapping induced by the defects in the thicker IZO layer.

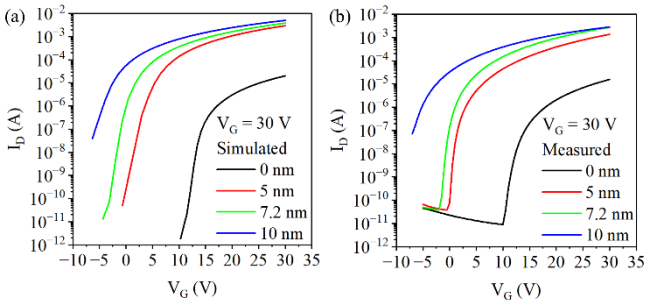

Fig. 3. Transfer characteristics of (a) simulated and (b) measured IZO/AIZO TFTs with a different IZO thickness.

The optimized device performance is achieved in TFTs featuring a 7.2 nm IZO/5.6 nm AIZO heterojunction channel, exhibiting a mobility of 17.6 cm^2/Vs and a current on/off ratio of ~10^8. To evaluate the suitability of these devices for displays, both positive bias stress (PBS, V_G = +30 V) and NBIS (V_G = -30 V, under WLED illumination) tests were conducted, as shown in Fig. 4. The TFTs demonstrate a good stability, with threshold voltage shifts of +1.4 V and -2.47 V after 1800 s of PBS and NBIS, respectively. These results represent significant improvements compared to single channel TFTs, and might be further improved by passivating the top channel surface to minimize the effects of ambient air exposure.

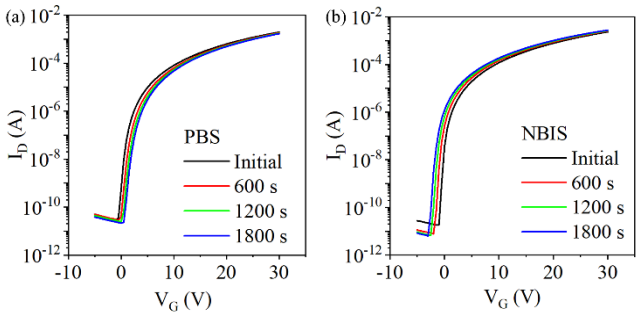

Fig. 4. Transfer characteristics of IZO/AIZO TFTs under (a) PBS and (b) NBIS conditions.

In summary, we investigated the effects of channel layer thickness on the performance of solution-processed heterojunction oxide TFTs through both computational simulations and experimental measurements. This work provides valuable insights into the design of high-performance oxide electronics and may contribute to the development of next-generation high-resolution, printable display technologies.

REFERENCES

[1] J. Wager, "Oxide TFTs: A Progress Report," Inf. Disp., vol. 32, no. 1, pp. 16-21, 2016.

[2] W. Cai, H. Li, and Z. Zang, "One-Volt, Solution-Processed InZnO Thin-Film Transistors," IEEE Electron Device Lett., vol. 42, no. 4, pp. 525-528, 2021.

[3] W. Cai, M. Li, H. Li, Q. Qian, and Z. Zang, "Significant performance and stability improvement of low-voltage InZnO thin-film transistors by slight La doping," Appl. Phys. Lett., vol. 121, no. 6, p. 062108. 2022.

[4] W. Cai, H. Li, M. Li, and Z. Zang, "Performance enhancement of solution-processed InZnO thin-film transistors by Al doping and surface passivation," J. Semicond., vol. 43, no. 3, p. 034101, 2022.

[5] Y. Zheng, Z. Wu, H. Tong, Z. Zang, and W. Cai, "Effects of La Doping on Persistent Photoconductivity of Solution-Processed InZnO Thin-Film Transistors," IEEE Trans. Electron Devices, vol. 71, no. 10, pp. 6061-6066, 2024.

[6] W. Cai, M. Li, S. Lu, Q. Qian, and Z. Zang, "Heterojunction Channel Engineering in Performance Enhancement of Solution-Processed Oxide Thin-Film Transistors," IEEE Trans. Electron Devices, vol. 70, no. 6, pp. 3085-3091, 2023.