Novel Variable Confinement SOAs Modelling

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Abstract - We have developed a numerical model for variable-confinement semiconductor optical amplifier (VC-SOA) operation which takes into account carrier recombination and loss mechanisms. It provides simulations of gain, noise figure and power saturation effects across different designs, serving as a valuable tool for device optimization.

Keywords - VC-SOAs, design, material engineering, simulation

I. INTRODUCTION

To meet the ever-growing demand for higher capacity in optical telecommunication networks, semiconductor optical amplifiers (SOAs) are promising due to their broadband optical gain. However, to achieve optimal performance, they require careful engineering of the active material and device design. In this context, novel variable confinement SOA architectures have been developed to locally adjust the active area to optical confinement ratio, enabling more efficient simultaneous optimization of gain, saturation output power (P_{sat}), and noise figure (NF) [1]. The numerical model presented enables accurate performance prediction and is validated against experimental data, positioning it as a reliable tool for the design of high-performance SOAs.

II. VARIABLE CONFINEMENT SOA MODELLING

The model we developed is based on M. J. Connelly's work [2] with appropriate modifications to tailor new multiquantum wells (MQWs) slab-coupled optical waveguide (SCOW) [3]. The energy levels are computed by solving the Schrödinger equation for a finite square potential well along the growth direction, assuming parabolic band dispersion in the in-plane direction for both conduction and valence bands [4]. The bandgap energy is derived from the active zone composition, taking into account strain and bandgap shrinkage effects. Subsequently, the carrier density, quasi-Fermi levels, Fermi-Dirac distribution functions, and the material gain coefficient are numerically calculated for MQWs structures. The travelling-wave equations are solved for the SOA discretized into spatial slices, taking into account the non-uniform carrier density distribution. Thus, amplified spontaneous emission (ASE) powers, gain, noise figure and saturation output power are extracted under steady-state conditon. For further details on the model, refer to [4] and herein references.

The novel variable confinement structures are 4-mm long and feature an active layer of thickness *d* composed of four compressively-strained $Ga_{0.196}In_{0.804}As_{0.784}P_{0.216}$ QWs grown by gas source molecular beam epitaxy, engineered to emit across the C+L band. The design enables to bind multiple electron and hole energy levels and supports broadband emission in the Transverse Electric (TE) polarization mode. This TE dominance arises from strong electron-to-heavyhole transitions and is further enhanced by the asymmetric cladding of SCOW structures [3]. To this architecture, we add a high-confinement (HC) region thanks to a p-doped highindex upper layer, which pulls the optical mode towards the quantum wells, enhancing optical confinement Γ in the active area. This layer is etched in tapers at the edges to gradually reduce the optical confinement, thereby forming the low-confinement (LC) regions (Fig. 1). The waveguide width *w* is also increased at the ends, enabling a transition from a low $d.w/\Gamma$ ratio in HC regions to a high ratio in LC regions.



Fig. 1. Variable confinement SOA and investigated design variants.

The model has been adjusted to account for optical confinement, waveguide width and loss coefficient α variations along the simulated devices. The designs are simulated using the Fimmprop software (PhotonDesign) to extract the optical confinement along the SOA. Variations in waveguide width are implemented into the model and tailored to each specific simulated structure. Finally, intrinsic losses, approximated by fitting to the experimental data, are assumed to vary with Γ because the optical mode is shifted away from the lossy upper p-cladding in LC sections. Nevertheless, intrinsic losses remain one of the most uncertain parameters in the model, though it still allows meaningful trend analysis. According to the literature, Γ/α_0 remains nearly constant along the structure - a condition that was applied in this work [1].

III. VARIABLE CONFINEMENT SOA DESIGN STUDY

As depicted in Fig. 1, the fabricated structures feature a 3.5-µm-wide waveguide, flared to 5 µm at both ends. The high-index upper layer extends over 50% or 75% of the SOA length and is positioned centrally. We first measure and simulate the gain spectra and NF of the 75% (green) and 50% HC (orange) regions designs at 700 mA, along with a reference SOA with a constant 5-µm wide waveguide and without HC region - referred to as the LC SOA (blue). Both experimental and calculated results are reported in Fig. 2.

The model accurately predicts the gain trend of these variable confinement designs, with the highest measured onchip gain (33 dB) obtained for the 75% HC design at 1580 nm - 10 dB higher than the standard LC design gain. However, the measured gain spectra of both HC designs are narrower than simulated, likely due to thermal effects arising from device heating at high gain levels. This discrepancy is particularly pronounced in the 75% HC design.



Fig. 2. Measured (solid line) and calculated (dashed line) small-signal chip gain and NF of the 3 designs biased at 700 mA.

Furthermore, the simulated and experimental NF values are in fairly good agreement. But, it is more challenging to accurately simulate the NF given the various influencing factors, especially propagation losses, and differential gain. The measured NF of the LC SOA (blue line) appears higher despite its lower Γ , which should typically reduce losses by reducing the optical mode confinement in the lossy p-doped cladding. This is likely due to the lower gain level. On the other hand, the model predicts that the 75% HC design should exhibit a lower NF than the 50% HC design due to its longer HC section enhancing the material gain when the measurements show no significant differences. This discrepancy could be due to an underestimation of losses potentially higher than simulated in the HC regions due to the upper p-doped layer - and/or the lower measured gain compared to simulations, due to heating effects. Moreover, under the same operating conditions, the simulated P_{sat} has been confronted with experimental results an reported in Fig. 3. The simulated data are in very good agreement with the measured results. The P_{sat} of the 50% HC design is slightly higher than the one of the 75% HC design, consistent with the model's prediction at 700 mA and 1580 nm. Additionally, the LC SOA P_{sat} was measured to be 18.5 dBm, near the simulated value of 19 dBm, which is higher than that of both VC-SOAs designs, as expected due to its higher active area to optical confinement ratio $(d.w/\Gamma)$.



Fig. 3. Measured (solid line) and calculated (dahsed line) chip gain and NF of the 3 designs at 1580 nm and 700 mA.

For a standard SOA, Γ can be adjusted through material engineering to achieve a given chip gain, and corresponding P_{sat} and NF. In fact, the $d.w/\Gamma$ ratio is minimized for a HC-type SOA with a constant A-cross-section and maximized for

a LC-type SOA with an B-cross-section (Fig. 1). Both exhibiting its own specific performance characteristics. However, in a complete VC-SOA structure with both HC and LC-type cross-sections, predicting performances becomes more complex and can be assisted by modeling. In Fig. 4.a. simulations using the developed model indicate that varying the ratio of the HC section length results in very little P_{sat} and NF variations at a given current (700 mA), with only a slight P_{sat} increase observed when the HC section length is reduced, but leading to gain degradation (Fig. 4.b).



Fig. 4. Chip Psat, NF (a) and gain (b) vs. HC ratio of a symmetric VCSOA.

The VC-SOA design will therefore require LC sections to improve Psat compared to the HC SOA exhibiting lower values compared to the LC SOA, combined with a HC section to improve chip gain level and NF. Thus, the HC section must therefore be long enough to obtain the desired level of gain at a given current (700 mA in Fig. 4) and can be easily chosen since both P_{sat} and NF value vary only slightly with HC section length for this design. The goal is to achieve the needed gain level at a reasonable injection current to reduce power consumption. In this respect, the model proves to be very useful for VC-SOA design, as it allows simulation of both material and geometric parameters along the device. Further work will consider asymmetric designs where the HC section is shifted toward the SOA input facet to evaluate its impact on the overall NF. Indeed, this positioning can be critical, as noise generated near the input is further amplified along the device.

IV. CONCLUSION

In this work, we presented a numerical model for gain, NF and P_{sat} operation of novel VC-SOA architectures. The model developed accurately reproduces key performance trends, making it a valid tool to assist future SOAs design.

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