

Machine learning enhanced design optimization and knowledge discovery for multi-junction photonic power converters

Karin Hinzer
SUNLAB
University of Ottawa
Ottawa, Canada
khinzer@uottawa.ca

Robert F. H. Hunter
SUNLAB
University of Ottawa
Ottawa, Canada

Gavin P. Forcade
SUNLAB
University of Ottawa
Ottawa, Canada

Yuri Grinberg
Digital Technologies Research Centre
National Research Council Canada
Ottawa, Canada

D. Paige Wilson
SUNLAB
University of Ottawa
Ottawa, Canada

Meghan N. Beattie
SUNLAB
University of Ottawa
Ottawa, Canada

Christopher E. Valdivia
SUNLAB
University of Ottawa
Ottawa, Canada

Mathieu de Lafontaine
SUNLAB
University of Ottawa
Ottawa, Canada

Louis-Philippe St-Arnaud
SUNLAB
University of Ottawa
Ottawa, Canada

Oliver Höhn
Fraunhofer Institute for Solar Energy
Systems
Freiburg, Germany

David Lackner
Fraunhofer Institute for Solar Energy
Systems
Freiburg, Germany

Carmine Pellegrino
Fraunhofer Institute for Solar Energy
Systems
Freiburg, Germany

Jacob J. Krich
SUNLAB
University of Ottawa
Ottawa, Canada

Alexandre Walker
Quantum and Nanotechnologies
Research Centre
National Research Council Canada
Ottawa, Canada

Henning Helmers
Fraunhofer Institute for Solar Energy
Systems
Freiburg, Germany

Abstract—We compare some classical and machine-learning enhanced design optimization methodologies. We investigate the design of the complex structures of ten-junction InP lattice-matched photonic power converters with $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ absorbers optimized for operation at 1550 nm with $53.6\% \pm 1.3\%$ conversion efficiency. We find that the implicit pattern recognition capabilities of dimensionality reduction using principal component analysis accelerates design discovery, optimization, and the understanding of complex optical phenomena in the simulated devices.

Keywords—machine learning, dimensionality reduction, design discovery, optimization acceleration, knowledge discovery, multi-junction photonic power converters

I. INTRODUCTION

Free-space and fiber-based optical links with photonic power converter (PPC) receiver elements offer the potential for fast, flexible, high-fidelity data and power transmission. We target novel high-efficiency ($\geq 50\%$) and high output voltage (≥ 5 V) 10-junction PPCs using InGaAs absorbers lattice-matched to InP for operation in the 1550 nm telecommunications C-band. The design landscape of these devices is high-dimensional and highly correlated. We leverage the pattern recognition capabilities of dimensionality reduction and machine learning algorithms, alongside classical optimization, to efficiently explore the design space of our PPCs. The wider survey that the machine-learning enhanced methods allow empowers a more informed design choice, where growth considerations and other criteria help select from the multiple high-performance designs that may

exist. We calibrate our device model with fabricated devices. We study the role of luminescent coupling in device performance. And, we investigate the potential for our machine learning enhanced methodology to expand the design perspective and supplement understanding of the design space for on-substrate multi-junction PPCs and those employing flat back-reflectors [1-4].

II. RESULTS AND DISCUSSION

We designed and grew lattice matched 1-junction photovoltaic (PV) samples by metalorganic vapor phase epitaxy on p-InP substrates at Fraunhofer ISE. For testing purposes thin absorbers of different thickness were grown and fabricated: 60, 180, and 540 nm. The absorber layer is sandwiched between higher bandgap front surface field (FSF) and back surface field (BSF) layers. We developed an optoelectronic model to simulate the PV devices using a drift-diffusion model in Synopsys Sentaurus TCAD software. Our 1-dimensional model treats the devices as laterally infinite layered structures.

The root-mean-square difference between measured & simulated EQE is within 1%, which supports our method of extracting the extinction coefficient for InGaAs. These 1-junction devices converted 1540 nm laser light with 2.66 W/cm^2 input power into electrical power at 2%, 5%, and 14% efficiency, for the 60 nm, 180 nm, and 540 nm devices, respectively. Using optimization techniques, we predict a maximum efficiency of 46% for an absorber layer thickness of 4380 nm and input power of 2.56 W/cm^2 . We fabricated 2- & 10-junction devices, which consist of InGaAs cells

connected in series with transparent tunnel diodes. We measured fabricated 10-junction InGaAs photonic power under 1.52 μm laser illumination at room temperature and observed a maximum efficiency of $46.4 \pm 1.6\%$ with an output power density of 16 W/cm^2 , a voltage output at maximum power of 5.01 V, and an open circuit voltage of 5.78 V. We will show fitting results of our model to these multi-junction devices, which include a detailed model of luminescent coupling between subcells & 10-junction optimization results.

We quantify the impact of luminescent coupling on device performance by calculating the coupling between each emission and absorption event using a transfer matrix method. For a test 2-junction structure, up to 85% of the emission events in the InGaAs absorber layers are re-absorbed within the device. This number increases to 96% when a planar back-reflector is included due to improved light management.

To further improve device efficiency using back reflectors, we have developed a computational framework employing Python and standard libraries to explore optoelectronic device design using machine learning. For our analysis, we apply principal component analysis as a dimensionality reduction technique. Dimensionality reduction enhanced optimization uses an optical model based on rigorous coupled wave analysis to produce current-matched subcells. Full efficiencies are determined by coupling to a drift-diffusion solver, with luminescent coupling. Fig. 1 illustrates the principal computational steps.

We find that for on-substrate 10-junction PPC devices, the absorber thicknesses converge to a unique optimum, which varies slightly ($\leq 5\%$) but systematically from Beer-Lambert expectations. For 10-junction devices with a flat Au back-reflector, the design space is richer, with a continuous subspace of similar performance optima with total absorber thicknesses varying by up to 25%. The optimization figure of merit (FOM) is defined as

$$\text{Photocurrent FOM} = \frac{\text{device photocurrent} [\#e]}{\text{incident photons per subcell} [\#\gamma]} \quad (1)$$

The optical generation current in number of electrons is divided by one-tenth of the input power, in number of photons,

as it is shared over the 10 subcells or segments of the device. The maximum value is 1. Optimized results display photocurrent FOM above 0.9925.

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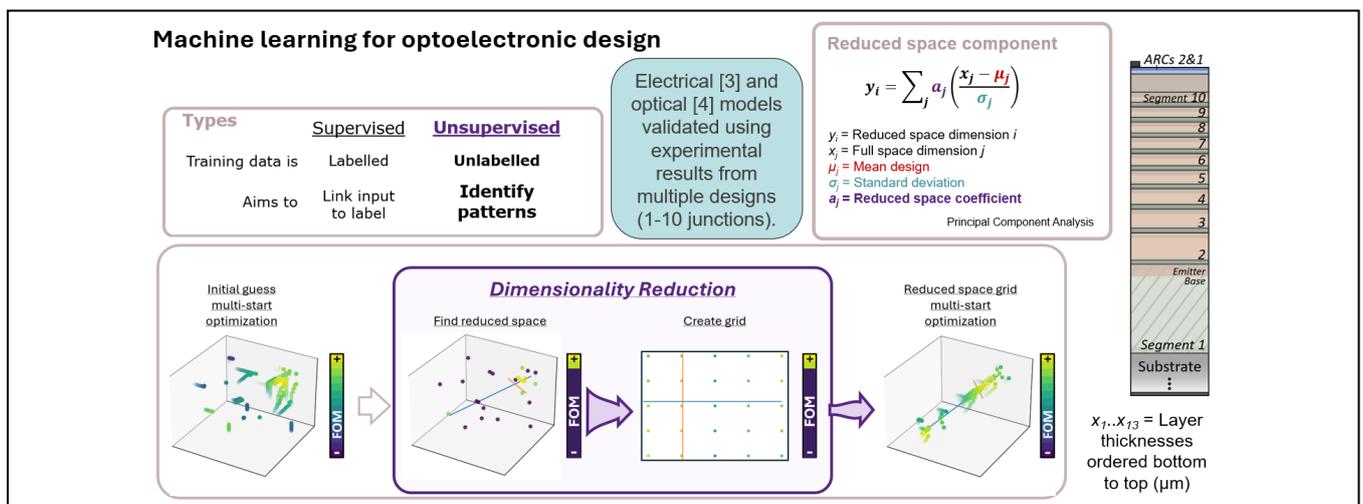


Fig. 1. Top: Results presented are generated using unsupervised machine learning with principal component analysis. Simplified schematic of the modeled on-substrate photonic power converter devices. Bottom: Simplified design flow for the machine learning enhanced design optimization. Step 1; classical multi-start optimization. Step 2; top designs from step 1 according to a chosen figure of merit (FOM) are used to train a dimensionality reduction algorithm and generate a reduced dimension subspace. Step 3; the reduced dimensional subspace is used to generate start points. Step 4; extension of the method, classical multi-start optimization from the step 3 grid points to mitigate information loss during steps 2 and 3.