Improving DBR operation at cryogenic temperatures through mirror grading

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***Abstract*— An investigation of different interface profiles of Distributed Bragg Reflectors (DBRs) operating at very low temperatures is developed. A thermal and electrical analysis showed an improvement of 66% at 20K chamber temperature in vertical resistance when implementing a uniparabolic grading at the hetero-barrier interfaces with respect to the step-like interfaces p-doped DBR.**

***Keywords*— cryogenic temperature, Distributed Bragg Reflectors, VCSEL, laser**

I. Introduction

A new breakthrough in data transfer technology has been reported [1], involving a Vertical-Cavity Surface-Emitting Laser (VCSEL) that operates at an ultra-low temperature of 4.2 K [2]. One of the key challenges encountered in optimizing the VCSEL's performance is the presence of potential barriers in the p-type DBRs, which significantly limit its capabilities [3]. The situation worsens as the temperature drops too much (cryogenic temperatures), where the carriers (specifically, the holes in the p-DBRs) lack sufficient thermal energy to surpass the potential barriers existing at the interfaces of the DBRs.

In this study, our aim is to address the potential barrier challenge by incorporating parabolic grading techniques at the interface of a hetero-barrier. To begin, it is essential to ascertain the actual operating temperature of the DBR within the 4.2K or any other chamber temperature. Subsequently, we explore the behavior of the DBR's I-V curve at various temperatures by introducing a graded mirror, comparing its performance with a p-doped DBR comprising of two step-like intermediate layers.

II. Theoretical Thermal Analysis of the DBR

When the current passing through the DBRs, heat is produced due to nonradiative recombination, and mainly by Joule heating; therefore, virtually all the input electrical power could be considered as being converted to heat [4]. So, we can extract an approximation for the heat source value from our experimental measurement of these DBRs. We measured the I-V curve with a pulse current of 1kHz with 5% duty cycle (i.e., the current injected into the device around 50µs). In Fig. 1, it can be seen that the temperature of a DBR put in a 4K and 20K chamber rises to 25K and 42K respectively in less than 15µs.

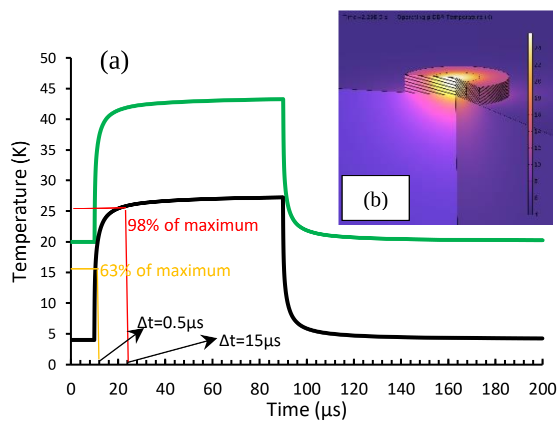

Fig. 1. (a) Time dependency of an operating p-DBR shows a 500ns temperature time constant and 15µs rising time and roughly 21K difference between operating and non-operating device. (b) A schematic picture of an operating p-doped DBR that is thermally insulated from the top side (thermal radiation is assumed to be small compared to thermal conduction) and contacted to the cryogenic plate from the bottom of substrate. The substrate height is 300µm, mesa height, mesa radius, and the aperture sizes are 3.38µm, 10µm, and 4.5µm respectively.

Now we know that the device temperature rises to higher values than the cryogenic chamber temperature itself shortly after we turn it on and sooner than the pulse width which means that the operating temperature is roughly 21K higher than the turned-off device. Therefore, we can calibrate our simulation with this temperature difference between operating and non-operating device.

III. Device Structure

The p-DBR was formed of 26 pairs of p-$Al_{0.12}GaAs$ high-index and p-$Al_{0.9}GaAs$ low-index layers with 130nm thickness for each period. Two different designs for the hetero barriers are considered: first one consists of two interface layers of 10nm steps with Al mole fraction of 0.25 and 0.71 respectively. The second considered structure is made of a 35nm uniparabolically graded layer with modulation doping to compensate the valance band potential barriers [5, 6].

IV. Device Performance and Results

The band-gap diagram of these two structures is shown in Fig. 2a and Fig. 2b. This band diagrams are simulated in COMSOL Multiphysics.

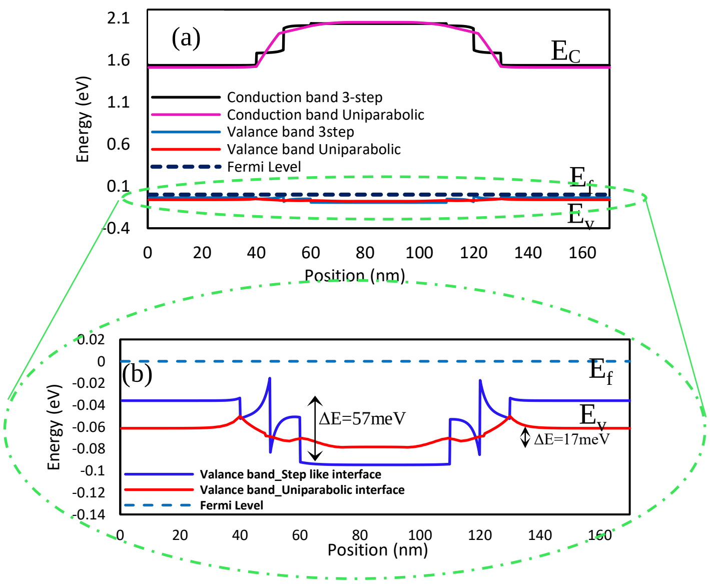

Fig. 2. (a) Band diagram of one period of a p-DBR one is uniparabolically graded and the other one utilize step interface. (b) zoomed view of the valance band of two structures.

In Fig. 2, the valance band kinks are mitigated due to the graded mirror's interface and modulation doping which result in lower potential barriers and higher current at lower temperatures. The I-V curves related to these two structures at different temperature are depicted in Fig. 3. It can be seen from both figures that at high temperatures, because the carriers have enough thermal energy (kT), they can easily flow in the device; but as temperature decreases, the carriers do not have enough thermal energy to surpass barriers thermally.

However, the carriers can still utilize intraband tunnel effect to move through the barriers even at low temperatures.

The graphs show that the series resistance of the p-DBR with uni-parabolically grading is improved three times at 20K (this is the least temperature we could reach due to convergence issues) chamber temperature (i.e., the operating temperature based the thermal analysis is roughly 41K) which is very critical because we need our VCSEL works very efficiently in the cryogenic environment. The I-V curves were simulated with Harold.

Conclusion

We estimated that the operating temperature of a p-DBR working at different cryogenic temperature environment, is 21K higher than its non-operating counterpart. We simulated a uniparabolic grading at the interfaces of a p-doped DBR. Results show that by properly designing the p-DBRs, which are the main source of series resistance in the VCSEL, the series resistance can be improved by 66% at the 20K temperature.

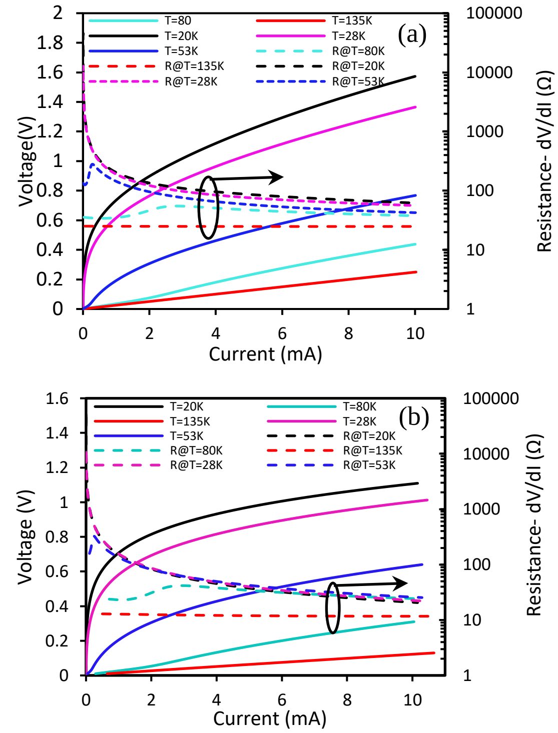

Fig. 3. (a) The lines show voltage versus current for a p-DBR with step-like interfaces and the dash-lines are representing the derivatives (resistance) and (b) depicts the uni-parabolically graded I-V and resistance curves.

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