Design and Optimizing Backside Grating Couplers in Si-Photonics Circuits

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***Abstract*—Grating couplers are essential in photonic systems, facilitating efficient light coupling between optical fibers and on-chip waveguides and allowing for wafer-level testing. With the increasing integration of photonics in communication systems like the internet, there is a growing need for grating couplers to be utilized on the backside of the chip, in addition to the top side. This paper presents a novel design for backside grating couplers by optimizing Si overlay on conventional grating couplers on silicon photonics circuits. The designed backside grating coupler simulation shows the coupling efficiency from the waveguide toward the back side is around 90% with reflection less than 2 %.**

***Index Terms*—Grating coupler, optical interconnects, Si-photonics.**

I. Introduction

In photonics and optical communication, grating couplers and edge couplers play vital roles in efficiently interfacing optical fibers with integrated photonic devices. They offer distinct approaches to facilitate efficient light coupling between waveguide modes and fiber mode (or free-space). While they share the common objective of light coupling, they differ in terms of their underlying principles, design considerations, and performance characteristics [1]. Grating couplers are based on the concept of utilizing a periodic grating structure to couple light between a waveguide and a free-space optical mode. This approach takes advantage of the diffraction phenomena to efficiently couple light from one medium to another. Grating couplers are typically fabricated by etching or depositing a periodic grating pattern on the surface of a waveguide [2]. The grating structure interacts with the incident light, diffracting it into the waveguide mode. Grating couplers offer advantages such as high coupling efficiency, a broad wavelength range, the ability to enable wafer-level testing, compatibility with standard fabrication processes, and the added benefit of relatively relaxed alignment tolerances to standard single-mode fiber. Also, grating couplers demonstrate a higher level of alignment tolerance with standard single-mode fiber. They find widespread applications in integrated photonic circuits, fiber-to-chip coupling, and on-chip optical interconnects [3]. On the other hand, edge couplers, also known as edge-coupled waveguides or butt-coupled waveguides, rely on the physical alignment of a waveguide edge with an optical fiber for efficient light coupling. Unlike grating couplers, edge couplers do not involve any diffractive elements. Instead, they rely on the precise alignment of the fiber mode and the waveguide mode. This alignment is achieved by bringing the waveguide and the fiber into close proximity, allowing the evanescent field of the waveguide mode to couple into the fiber mode [4].

The focus of this paper revolves around the backside grating coupler, a specific type of grating coupler designed to direct light toward the back of the chip rather than the top side. Backside grating couplers have emerged as a significant component in Si-photonics. The most important advantage of backside grating couplers is that they free up the top side of the chip, which is not used for optical coupling. This opens up additional space and flexibility in the packaging design, allowing for the integration of other components or functionalities on the topside of the chip [5].

II. Design and Simulations

In Si-photonics, shallow etching on silicon waveguides is a commonly employed technique for creating grating couplers. Adding a Si-overlay on the waveguide is utilized to enhance the efficiency of the coupler [6]. Fig.1 illustrates a novel geometry of the grating coupler with the help of a Si-overlay.

The proposed idea involves creating a waveguide using Si-overlay and transmitting light to Si-overlay. On the other hand, by etching on the Si waveguide, the grating is formed, and light is diffracted to the back side. It appears to be mirrored horizontally compared to a normal grating coupler. Compared to the previous bake side grating coupler [5], in the new design, the metal mirror is no longer required. Removing the metal mirror has resulted in cost reduction and simplified

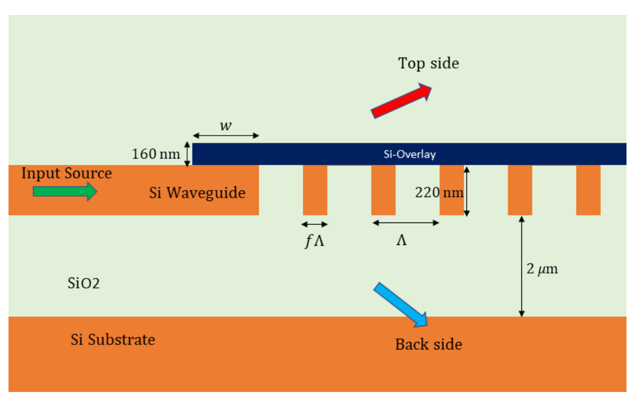

Fig. 1. The geometry of grating coupler.

manufacturing processes. Additionally, the new design can be implemented in passive fabrication that usually do not involve any metal deposition in their processes.

The symbol Λ denotes the grating pitch, while the symbol f represents the grating's fill factor, which is achieved by etching the Si waveguide. The variable w represents the width of the overlap region between the waveguide and the Si-Overlay. The grating consists of 60 repeating pitch units.

The behavior of a grating coupler is simulated using the 2D Finite-Difference Time-Domain (FDTD) method [7]. The simulations are performed at a specific wavelength of 1550 nm. Three monitors are utilized to observe the optical power ratios to ensure a fair comparison of light intensity. These ratios include the power transmitted from the input to the top side (T_{Top}), the power transmitted from the input to the back side (T_{Back}), and the ratio of reflected light to the input power (R). This width plays a crucial role in controlling the reflection of the input. To determine the optimal value of w, a parameter sweep is performed over a range of 0 to 1.5 μm, while keeping the Λ constant at 620 nm and the f at 0.35(Fig.2). According to the results, the optimal value for w is 0.8 μm. Another sweep parameter involves varying the Λ and f to maximize the T_{Back} while keeping the w constant at 0.8 μm. Based on the results shown in Fig.3, the best performance is achieved when the Λ = 660 nm and f=0.3.

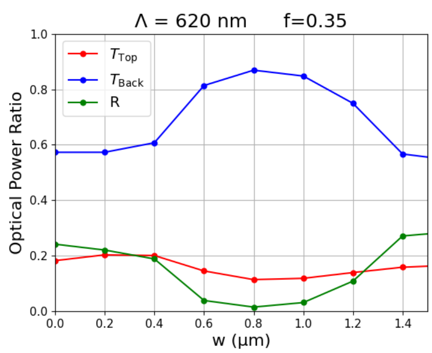

Fig. 2. The optical power ratios for different values of w

III. Result and Discussion

The optimal parameters are Λ = 660 nm, f=0.30 and w=0.8 μm. The proposed backside grating coupler demonstrates a high T_{Back} value around 90 %, while T_{Top} and R are less than 8 % and 2 %, respectively. Additionally, Fig.4 illustrates the magnitude of the Electric fields(E) profile. It is important to note that these results are obtained while considering the feature size limitation during fabrication. If the feature size limitation is not considered, it is possible to achieve even better results. Furthermore, there may be additional losses because of coupling between the backside of the chip (Si substrate) and the fiber optic, which are not taken into account in simulations.

IV. Conclusion

In conclusion, this study introduces a novel approach to integrating backside grating couplers in Si-Photonics circuits.

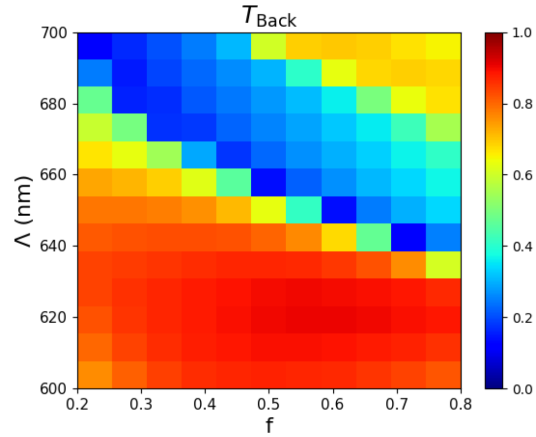

Fig. 3. The T_{Back} for different values of Λ and f at w=0.8 μm

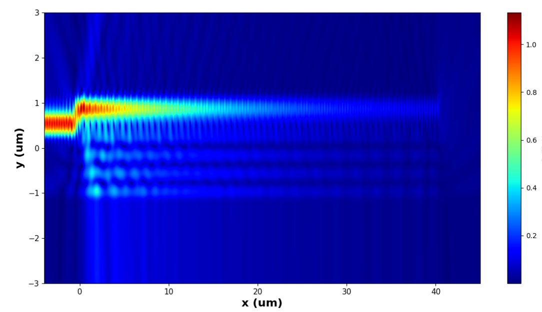

Fig. 4. The E over x and y.

Given the growing need for efficient light coupling in photonics systems, the utilization of grating couplers on the backside of the chip has become increasingly important. By precisely adjusting key physical parameters such as pitch and filling factor, the direction of light can be effectively controlled towards the backside of the chip.

Acknowledgment

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