Identifying Defects in Charge Trapping Related Phenomena

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***Abstract*—Charge trapping at oxide defects is a prevalent phenomenon in most modern nanoelectronic devices, leading to detrimental reliability issues like bias temperature instability (BTI), trap-assisted tunneling (TAT) or random telegraph noise (RTN). Although these effects are clearly visible in experiments, the microscopic nature of the involved defects remains elusive. However, an in-depth understanding of the underlying atomistic processes and defects responsible for device degradation is key to further improve device reliability. In this work we discuss how insights gained from electrical characterization methods, ab-initio calculations based on density functional theory (DFT), and compact device models can be combined to identify defects near the semiconductor/oxide interface which compromise device reliability.**

***Index Terms*—Defects, random telegraph noise (RTN), bias temperature instability (BTI), device reliability**

I. Introduction

Nonradiative processes involving defects give rise to multiple detrimental effects in electronic devices. For instance, it is suspected that the well-known degradation of Si based solar cells is linked to breaking Si-H bonds at the Si/SiO_x interface [1]. This leads to the creation of Si dangling bonds, which act as efficient recombination centers through the nonradiative Shockley-Read-Hall process [2]. Furthermore, in MOSFET devices defects in the gate insulator can trap charges from the device, thereby channel leading to a fluctuation of charge in the insulator. In large-area devices this leads to a drift of the threshold voltage known as bias temperature instability (BTI) [3], whereas in ultra-scaled devices the same effect leads to discrete steps in the drain current caused by individual charge capture and emission events, known as random telegraph noise (RTN) [4]. In all these phenomena, the charge transfer from/to the defect is mediated by electron-phonon coupling and is hence temperature-activated. However, due to nuclear tunneling these effects can also persist at cryogenic temperatures and hence pose challenges for quantum computing applications, since the resulting charge noise limits the achievable coherence time of the quantum states.

Here we use a multi-scale modeling approach combining first-principles calculations with compact device models to reveal the microscopic nature of defects from electrical characterization techniques applicable to fully processed devices. We apply this methodology to identify defects responsible for RTN at cryogenic temperatures and leakage-currents in devices with a SiO_2 dielectric.

This work was in part funded by the European Union's Horizon 2020 research and innovation program under grant agreement No. 871813, within the framework of the project Modeling Unconventional Nanoscaled Device-FABrication (MUNDFAB).

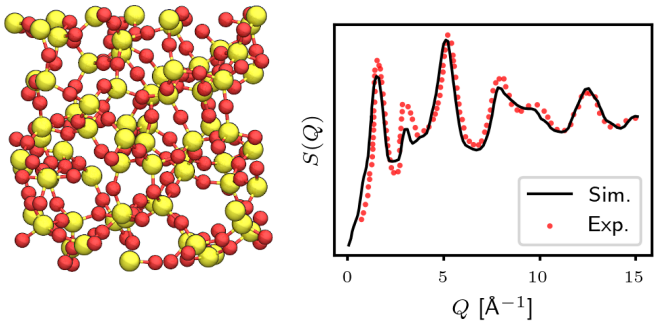

Fig. 1. **Left:** An example of an atomistic model structure for amorphous SiO_2 containing 216 atoms. **Right:** The validity of the atomistic models is verified by comparing the theoretical structure factor $S(Q)$ of the model to experimental data [5]. Adapted from [6].

II. Methodology

The theory of nonradiative multiphonon (NMP) transitions was pioneered already in the 1950s by Huang and Rhys [7] and was later refined by Henry and Lang [8]. However, quantitative parameter-free predictions of the transition rates for a given defect candidate only became possible rather recently by formulations of NMP theory suitable for first-principle calculations based on density functional theory (DFT) [9]. Here we employ DFT as implemented in the CP2K [10] code with a range-separated PBE0 hybrid functional [11] to calculate important defect parameters like the thermodynamic trap levels E_T and the relaxation energy E_R, which determine the charge trapping dynamics of a certain defect. In order to study defects in amorphous oxides or at the semiconductor/oxide interface, a realistic atomistic model for the host material is needed. We create such amorphous models with a melt-and-quench molecular dynamics simulation using empirical force fields like ReaxFF [12] or, more recently, with machine-learned potentials [13] trained on energies and forces from DFT for a particular material system. The validity of the model structures is then confirmed by comparing characteristic material properties like the structure factor $S(Q)$ to experimental data. One of the amorphous SiO_2 (a-SiO_2) structures used in this work is shown in Fig. 1.

While DFT provides fundamental insights to the defect physics, a macroscopic device model is needed to link the DFT results to electrically measurable effects on the device, e.g. a shift of the threshold voltage. Here we use our recently released compact device simulator *Comphy* [14], which is based on a physical description of charge trapping within NMP theory. Using this physics-based model, we can extract parameters like E_T and E_R from electrical device characterizations,

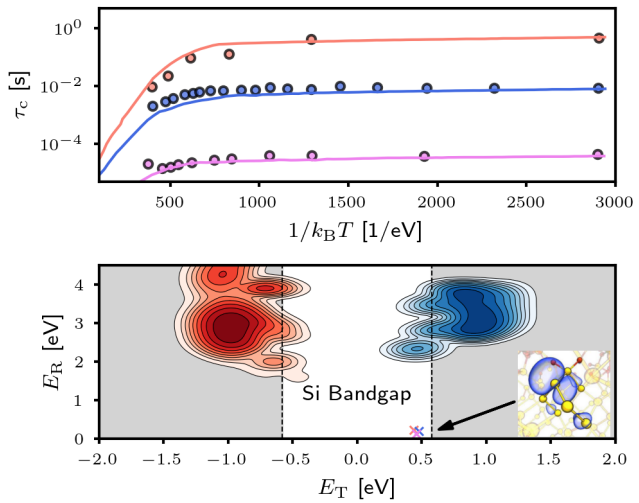

Fig. 2. **Top:** Experimental capture time constants τ_c for three defects (dots) as extracted from RTN measurements at cryogenic temperatures (4 K to 30 K) together with the corresponding model predictions (lines). **Bottom:** The required defect parameters (crosses) to describe the charge trapping behavior are vastly different from typical parameter distributions for hole (red) or electron (blue) traps in a-SiO_2 [18]. Instead, the observed defect parameters match the canonical P_b-center at the Si/SiO_2 interface (inset), making it a likely cause for noise in the studied devices. Adapted from [17].

e.g. measure-stress-measure (MSM) [15] procedures or RTN analysis [16], and compare it to theoretical predictions from *ab-initio* methods for a particular defect candidate.

III. Results

In our first showcase we study the origin of RTN in Si-based CMOS devices for controlling solid-state qubits at cryogenic temperatures. Reducing the noise level is critical here to increase the coherence time of the quantum states. In order to extract the defect parameters, we analyzed the capture and emission times visible in the RTN signal at various temperatures and gate biases, a detailed description is provided in [17]. As shown in Fig. 2 (top), the time constants do not follow an Arrhenius law and become constant towards cryogenic temperatures, which is a clear indication for a nuclear tunneling dominated process. Our analysis shows that the responsible defects have a relaxation energy of $E_R \approx 0.1\,\text{eV}$ with the $0/-$ trap level close to the Si conduction band. We previously extracted the parameter distributions of defects in a-SiO_2 responsible for BTI and determined that hydrogen-related defects like the hydroxyl-E' center or the hydrogen bridge are the root cause of BTI [18]. However, as can be seen in Fig. 2 (bottom), the distributions of these oxide defects are incompatible with the required parameters for the RTN defects, since oxide defects typically have much larger relaxation energies and as a result show a pronounced temperature dependence. Furthermore, the device simulations reveal that the defects have to be in close proximity to the Si/SiO_2 interface. By comparison of our model parameters to ab-initio calculations in explicit atomistic models of the Si/SiO_2 interface [19], we find that the canonical P_b-center, i.e. a Si dangling bond at the interface, is a likely source of noise in the investigated devices at cryogenic temperatures.

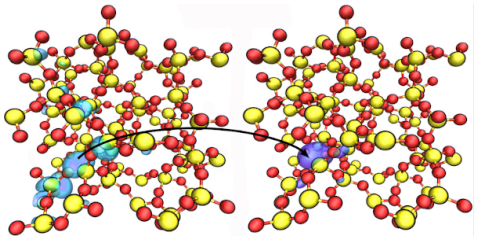

Fig. 3. **Left:** In a-SiO_2 and other amorphous oxides, the bottom of the conduction band is semilocalized around particular sites **Right:** Injected electrons can spontaneously localize at those sites and form a small polaron. Adapted from [20].

In another application of our multi-scale modeling approach, we investigate the leakage currents in SiC/SiO_2 MOSCAP devices [20]. The strong temperature dependence of the leakage currents in these devices hints at a trap-assisted tunneling (TAT) mechanism being responsible for the leakage. Here we determine the corresponding defect parameters by calculating the theoretical leakage current based on samples of a Gaussian parameter distribution [21] and comparison with the measured leakage currents. While in the case of TAT the responsible defects have to be located in the oxide, the extracted relaxation energy of $E_R \approx 1.0\,\text{eV}$ is still incompatible with most defects in a-SiO_2. However, the extracted parameters suggest a conduction mechanism via electron polarons, which is further supported by ab-initio simulations of intrinsic charge trapping in a-SiO_2 [20]. Here, electrons are not trapped in an actual defect, but rather spontaneously localize at particular sites within the a-SiO_2 as shown in Fig. 3.

IV. Conclusions

We showed that the microscopic nature of defects responsible for various detrimental effects on electronic devices can be revealed by combining first-principles approaches with macroscopic device simulations and experiments. While we demonstrated this approach for devices with a SiO_2 dielectric, this methodology can also be applied to identify relevant defects in emerging technologies like devices based on 2D materials.

References

[1] A. Diggs et al, *Commun Mater* 4, 24 (2023)
[2] S. De Wolf et al, *Phys. Rev. B* 85, 113302 (2012)
[3] D. K. Schroder, *Microelectronics Reliability* 47, 841–852 (2007)
[4] K. S. Ralls et al, *Phys. Rev. Lett.* 52, 228–231 (1984)
[5] D. Price, J. Carpenter, *J. Non-Cryst. Solids* 92 (1) 153–174 (1987)
[6] C. Wilhelmer et al, Microelectronics Reliability 139, 114801 (2022)
[7] K. Huang, A. Rhys, N.F. Mott, *Proc. R. Soc. Lond. Ser. A Math. Phys. Eng. Sci.* 204, (1078) 406–423 (1950)
[8] C.H. Henry, D.V. Lang, *Phys. Rev. B* 15, 989–1016 (1977)
[9] A. Alkauskas et al, *Physical Review B* 90, (7), 075202 (2014)
[10] T.D. Kühne et al, *J. Chem. Phys.* 152, 194103 (2020)
[11] M. Guidon et al, *J. Chem. Theory Comput.* 5 (11) 3010–3021 (2009)
[12] A. Van Duin et al, *J. Phys. Chem. A* 107 (19) 3803–3811, (2003)
[13] D. Milardovich et al, *J. Chem. Phys.* 158, 194802 (2023)
[14] D. Waldhoer et al, *Microelectronics Reliability* 146, 115004 (2023)
[15] B. Kaczer et al, IEEE IRPS 2008, pp. 20-27
[16] H. Miki et al, IEEE IEDM 2012, pp. 19.1.1–19.1.4
[17] J. Michl et al, IEEE IEDM 2021, pp. 31.3.1-31.3.4
[18] D. Waldhoer et al, *IEEE T-ED* 68 (8), 4057-4063 (2021)
[19] B. Ruch et al, *IEEE T-ED* 68, (4), 2092 - 2097 (2021)
[20] C. Schleich et al, *IEEE T-ED* 69, (8), 4486 - 4493 (2022)
[21] C. Schleich et al, *IEEE T-ED* 69, (8), 4479-4485 (2022)