Addressing the electrical degradation of 845 nm micro-transfer printed VCSILs through TCAD simulations

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***Abstract*—In this work we present the electrical modeling of novel 845 nm vertical-cavity silicon-integrated lasers (VCSILs) for silicon photonics (SiPh). We tested the reliability of the devices by submitting them to high current stress, corresponding to ≈ 20xI_{th}, to observe the degradation as a function of time. During the stress experiment, we monitored the electrical characteristics at regular intervals and we observed two separate degradation phenomena: the series resistance increment and the lowering of the turn-on voltage. Thanks to a Poisson-drift diffusion simulator we simulated the I-V characteristics and the band diagrams to interpret the degradation phenomena. The results of the simulations confirmed that the electrical degradation can be caused by the diffusion of compensation impurities originating from the p-contact layers. The same mechanism was also responsible of the optical degradation of the devices.**

***Index Terms*—Degradation, Impurities, VCSIL, Silicon photonics, Diffusion**

I. Introduction

Over the last decade, silicon photonics (SiPh) reached a huge development in terms of integration and complexity [1]. Moreover, SiPh expanded its portfolio of applications including not only datacom and telecom applications [2], but also sensors [3] and light detection and ranging systems (LIDARs) [4]. One of the key elements enabling SiPh to reach high compactness with reduced costs are low-loss silicon waveguides integrated into highly miniaturized optical systems manufactured through the conventional CMOS fabrication process. However, also laser diodes play a crucial role in photonic integrated circuits (PICs), since they are the light source of the entire chip. Indeed, vertical-cavity surface-emitting lasers (VCSELs) are usually employed in the 850-950 nm communication window for direct modulation in a variety of applications [5]. The devices under study are state-of-the-art vertical-cavity silicon-integrated lasers (VCSILs). Unlike common vertical-cavity lasers, which are grown and operate onto a native substrate, VCSILs are composed of a VCSEL grown on native substrate from which they are removed and then attached to a photonic circuit through the micro-transfer printing technique [6]. This method is highly effective in developing laser diodes for SiPh, it allows to integrate high-quality III-V active materials directly onto silicon substrates, thus overcoming the intrinsic limitations of Si and Si-based material systems in emitting light due to their indirect bandgap [7]. In this work, we studied the electrical degradation of 845 nm VCSILs. At first, we experimentally evaluated the degradation of the devices with a constant current stress experiment. By means of a commercially-available physics-based simulation suite we emulated the experimental kinetics related to the series resistance increment and to the lowering of the turn-on voltage. With the outcome of our analysis, we demonstrated that the observed electrical degradation originated from the diffusion of a compensating species migrating from the p-contact layers toward the active region, through the top DBR.

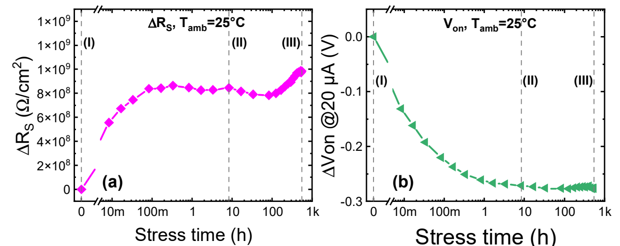

Fig. 1. Experimental characterization: (a) series resistance and (b) turn-on voltage.

II. Experimental results

The devices analyzed within this work are vertical-cavity silicon-integrated lasers emitting at 845 nm. Each device consists of a III-V VCSEL, designed for bottom-emission, with five 4 nm thick $In_{0.10}Ga_{0.90}As/Al_{0.37}Ga_{0.63}As$ QWs and $Al_{0.12}Ga_{0.88}As/Al_{0.90}Ga_{0.10}As$ DBR mirrors. A detailed and

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complete description of the devices (including the photonic platform) can be found in [8]. The stress and the electrical characterization were performed by means of an HP 4142 source-meter. The constant current aging test was carried out at T_{amb}=25°C with a bias of 3.5 mA (27.86 kA/cm^2) to observe the degradation kinetics in a reasonable amount of time (<550 hours). This represents a highly critical stress condition, as the unaged devices have a threshold current of ≈170 µA. By collecting the I-V characteristics at regular time intervals we observed two degradation phenomena: the increment in the series resistance (Fig. 1b) and the lowering in the turn-on voltage (Fig. 1a). We considered three relevant points of the series resistance kinetics: (I) unaged characterization, (II) end of the first series resistance increment and end of the turn-on voltage lowering, and (III) post-stress characterization, after the onset of the second series resistance increment.

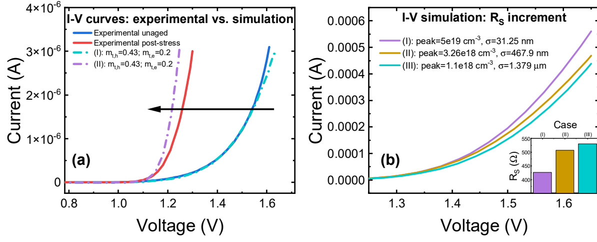

Fig. 2. Simulation results: (a) turn-on voltage anticipation and (b) series resistance increment (without the parasitic M-S junction).

III. Simulation Results

To interpret the experimental results, we employed a commercial simulator, Sentaurus TCAD, to emulate the two electrical degradation processes presented in the previous paragraph. According to our hypothesis, also supported by the results of the optical degradation, the worsening of the electrical characteristics is ascribed to the migration of impurities. These diffuse from the p-contact layers towards the active region and are capable of compensating the p-type dopants in the top DBR of the device. The results of the I-V characterizations showed two distinct series resistance increments (points (I) and (II)), and the lowering of the V_{on} which almost ends at point (II). Referring to the three conditions, indicated as (I), (II), and (III), we emulated the experimentally observed electrical degradation by imposing a specific distribution of compensating impurities. To match condition (I), we placed a Gaussian distribution of shallow donors close to the contact layers, which caused a potential barrier in the valence band (Fig. 3). For conditions (II) and (III) the distribution was changed according to the Fick's second law of diffusion [9]. In point (II) the compensating distribution increased the potential barriers in the valence band of the DBR, whereas in point (III) the variation of R_S is originated by the influence of the Gaussian tail in the proximity of the oxide aperture (Fig. 2b). Then, with the same process, we emulated the turn-on voltage decrease considering the p-contact as a metal-semiconductor (M-S) junction instead of an ideal contact. In the condition of point (II) we can simulate a consistent turn-on anticipation (Fig. 2a) since the lowering of the compensating impurities close to the p-contact lowers the barrier width for the tunneling in the parasitic M-S junction.

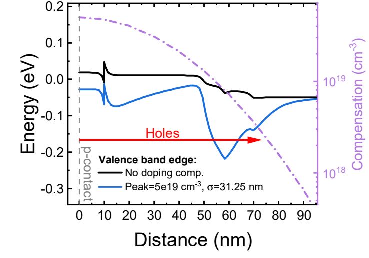

Fig. 3. Simulation of the valence band at equilibrium for case (I): the depicted potential barrier was found to increase the series resistance.

V. Conclusions

In conclusion, we evaluated the electrical degradation of novel VCSILs submitted to a constant current stress at 3.5 mA (27 kA/cm^2) at room temperature. The stress procedure induced a reduction in the operating voltage and an increment in the series resistance. By simulations, we were able to pinpoint the physical origin of degradation. In particular, both the observed variations in the electrical characteristics could be explained by considering the migration of compensating impurities originally located in the proximity of the p-side contact. Initially, the presence of these impurities originally caused a high V_{on} due to a parasitic M-S junction. With the stress these impurities start to migrate lowering the operating voltage and introducing potential barriers in the valence band which increment the series resistance.

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