Optimization of interdigitated back contact geometry in silicon heterojunction solar cell

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Abstract—In-house developed 2D semiconductor simulator ASPIN3 is used to simulate amorphous silicon / crystalline silicon heterojunction cells with interdigitated contacts on the back side. Our focus is on finding the optimal widths of emitter and back surface field stripes as well as the width of the gap between them. Analysis of the three dimensional parameter space reveals that high efficiencies can be achieved for relatively large widths, over 100 μ m, allowing the use of simple patterning techniques to create the cells.

I. INTRODUCTION

Amorphous silicon (a-Si:H) / crystalline silicon (c-Si) heterojunction solar cell (SHJ) technology is capable of reaching high open-circuit voltages due to excellent surface passivation of c-Si by the thin intrinsic a-Si:H layers. By moving the front contact to the back side of the cell in an interdigitated back contacted manner (IBC) the optical losses at the front of the cell can be drastically lowered, resulting in high short-circuit current densities. High open-circuit voltages and short-circuit currents of the IBC SHJ result in conversion efficiencies reaching over 25% [1], which are currently the highest efficiencies obtained with crystalline silicon technology.

In this simulation study we use in-house developed semiconductor simulator ASPIN3, capable of simulating optoelectronic heterostructures in two dimensions, to analyze the geometry of the contacts on the back side of the IBC SHJ cell. IBC studies in literature focus mostly on simultaneous variation of one or two parameters at most [2]–[4]. We use ASPIN3 to simultaneously vary three IBC parameters: the widths of the p and n doped stripes and the width of the gap between them.

II. MODEL DESCRIPTION

ASPIN3 is based on the Poisson's, transport and continuity equations. The generation rate profile, needed to simulate illuminated structures was calculated with Sun*Shine* optical simulator [5] using standard AM1.5 spectrum. The schematic representation of the simulated structure with layer thicknesses is shown in Fig. 1. For a-Si:H layers the distribution of states in the bandgap includes exponential tails below conduction and above valence band as well as a Gaussian distribution of dangling bonds, described in detail in [6]. Recombinations in *n*-type c-Si absorber include radiative, Auger and Shockley-Read-Hall (SRH) recombinations. Auger recombinations are modeled after parametrization of Richter [7]. Main input parameters are given in Table I.



Fig. 1. Schematic representation of the IBC SHJ solar cell with layer thicknesses. To limit the simulation domain we chose a symmetric section of the entire SHJ structure. Note that the varied widths in the simulation, W_p and W_n , correspond to half of the entire emitter and BSF stripe width respectively.

To find the geometrical configuration with highest efficiency we vary half of the emitter strip width W_p , gap width W_{gap} and half of the back surface field strip width W_n in range from 10 µm to 1 mm. For each configuration of widths a current-voltage curve is simulated from which the efficiency is evaluated.

III. RESULTS AND DISCUSSION

We ran the simulations for two different cases. In the first case we assumed an ideal cell with only intrinsic recombinations in the wafer (radiative, Auger) and perfect front surface passivation (0 surface recombination velocity).

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SIMULATION INPUT PARAMETERS				
	c-Si(n)	a-Si(i)	a-Si(n)	a-Si(p)
Dielectric constant	11.9	11.9	11.9	11.9
Electron affinity (eV)	4.05	3.9	3.9	3.9
Band gap (eV)	1.124	1.7	1.7	1.7
Effective conduction band density of states (cm ⁻³)	2.8×10 ¹⁹	2×10 ²⁰	2×10 ²⁰	2×10 ²⁰
Effective valence band density of states (cm ⁻³)	3.1×10 ¹⁹	2×10 ²⁰	2×10 ²⁰	2×10 ²⁰
Electron mobility $(cm^2 V^{-1} s^{-1})$	1324	10	10	10
Hole mobility $(cm^2 V^{-1} s^{-1})$	452	2	2	2
Acceptor density (cm ⁻³)	0	0	0	1×10^{18}
Donor density (cm ⁻³)	1×10^{15}	0	1×10^{18}	0



Fig. 2. Efficiency contour plots for wafer with radiative and Auger recombinations only. Contour plots are positioned at W_{gap} values of 10, 42, 237 and 1000 µm. Black triangles mark the position of the highest efficiency for each W_{gap} position.

Efficiency of the cell in this case is shown in Fig. 2 as a function of W_n , W_p and W_{gap} . Highest efficiency of 26.3% is obtained for $W_p = 100 \ \mu\text{m}$, $W_n = 10 \ \mu\text{m}$ and $W_{gap} = 10 \ \mu\text{m}$. Results show that large W_n and W_{gap} result in decreased efficiencies. This is due to increased average lateral distance that minority carriers have to travel to reach the emitter. Increasing W_p results in increasing efficiencies at first, which is more pronounced for large W_{gap} or W_n , followed by a decrease. Minority carriers generated over the emitter region do not need to travel laterally, resulting in higher efficiencies for wider emitters. Wider emitters also increase the length that the majority carriers have to travel to reach the BSF increasing the series resistance. Once series resistance is large enough a drop in efficiency occurs. Overall the variation of efficiency with W_p is smaller than with W_n or W_{gap} . The results show that high efficiencies can be achieved for relatively large widths. Efficiency over 26% can be realized with all of the widths over 100 µm, allowing the use of simple patterning techniques.

In the second case we simulated a more realistic cell and introduced SRH recombinations with minority carrier lifetime of 5 ms and a front surface recombination velocity of 5 cm/s. Results are shown in Fig. 3. Overall efficiency of the cell is lower as in the first case. The highest efficiency reaches 24.3%, but the optimal widths stay the same as in the first case, indicating that the optimal geometry configuration is independent from the wafer and passivation quality, at least for high efficiency IBC SHJ cells.

IV. CONCLUSION

We have demonstrated the use of ASPIN3 semiconductor simulator to explore a three dimensional parameter space of doped stripes and gap widths of the IBC SHJ cell. Instead of only searching for the optimal geometry configuration we



Fig. 3. Efficiency contour plots for wafer with SRH recombinations and nonzero front surface recombination velocity. Contour plots are positioned at same W_{gap} as Fig. 2. Black triangles mark the position of the highest efficiency for each W_{gap} position.

present a full parameter space exploration. We analyzed two different cases of wafer lifetime and front surface passivation, giving better insight into the sensitivity of efficiency to each varied parameter.

V. ACKNOWLEDGMENTS

The authors acknowledge the financial support from the Slovenian Research Agency (Research Programme P2-0197), Ministry of Education, Science and Sport and European Social Fund (Project M-1329E).

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