Scaled III-V optoelectronic devices on silicon

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***Abstract*—In the present talk we discuss the development of the epitaxial technique Template-Assisted Selective Epitaxy (TASE) and its application for the monolithic integration of scaled III-V active photonic devices on silicon.**

A unique advantage of TASE for silicon photonics applications is that it enables a truly local integration of III-V material at precisely defined positions, it is therefore particularly suited for densely integrated nanophotonic devices.

Here we will discuss our work on InP-based microdisk lasers fabricated by either direct TASE growth or via the use of micro-substrates. Optical mode simulations using Lumerical are used to explore the design space.

Notably, we are exploring the use of metal-clad cavities for further light confinement. The metal-clad cavities enable scaling of the laser diameter beyond what is achievable with a pure photonic cavity. Thermal simulations are used to explore the impact of the metal-cladding as a heat sink as opposed to plasmonic operation. We also evaluate the potential for electrical actuation and will show first results on monolithic photodetectors, using Sentaurus simulations to improve our understanding of device performance.

I. Introduction

The advanced state of silicon processing technology makes it ideally suited as a platform for silicon photonics. Silicon is the material of choice for electronics and we can look back on more than 60 years of CMOS processing technology. The advanced processing technology together with the high index contrast enables the fabrication of low-loss silicon waveguides with a high degree of confinement. Silicon is transparent above 1.1 µm wavelengths which makes it useful for detectors in the visible region, but the indirect bandgap prevents the implementation of lasers or LEDs. Despite sustained efforts on group-IV light sources, III-V remains the best solution because of the direct and tunable bandgap of many of its compounds, which enables the implementation of complex photonic structures.

The integration of III-V material or devices on silicon has therefore been a long-standing goal for the development of a complete optoelectronic link – waveguide, detectors and emitters on the same chip [1,2]. However, due to both lattice- and thermal mismatch direct growth of high-quality III-V on silicon is non-trivial.

To address this challenge our group pioneered the Template-Assisted Selective Epitaxy (TASE) approach, which does away with many of the limitations of traditional NW growth with respect to device fabrication, such as overgrowth of junctions and limitations with respect to orientation or geometry. Initially we were exploring electronic applications [3,4], but more recently we have been expanding into the world of photonics.

II. Device Fabrication

The main concept of TASE relies on the use of a single seed combined with guided growth of III-Vs within a confined oxide template, as illustrated in Fig. 1. At one extremity of the template there is access to silicon to start the nucleation, and subsequently it is the template which guides the growth progression. This decoupling of the resulting geometry from the growth mode and substrate orientation, results in a larger processing window as well as a number of other advantages.

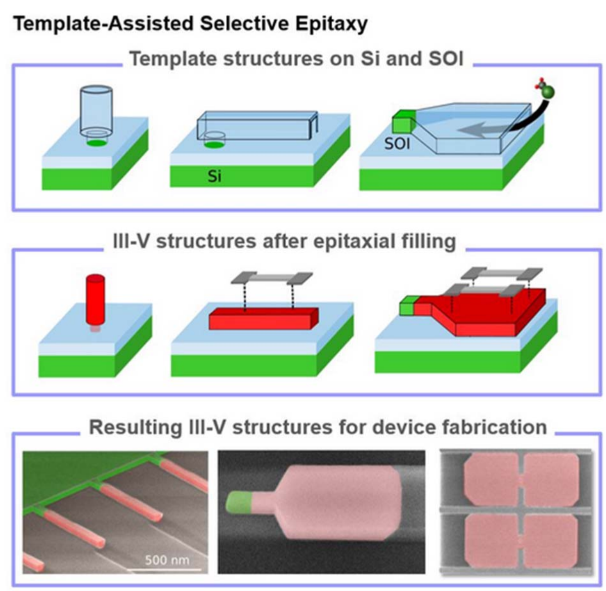

Figure 1 schematics showing the concept of TASE before and after III-V filling of templates and below top-view SEM images of some examples of III-V crystals.

A unique advantage of TASE for silicon photonics applications is that it allows for the truly local integration of III-V material at precisely defined positions, since the location of the III-V may be defined with nm-scale position in the same lithographic step. Compared to other techniques this therefore

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in principle enables relatively easy co-integration with silicon passives and electronics.

Therefore, we have been exploring the direct monolithic growth of GaAs [5,6] and InP [7] microdisk lasers on silicon. These devices show optically pumped lasing around 840 - 870 nm. We compared the InP devices with identical structures based on wafer bonding and found that at room temperature TASE samples show very similar behavior to bonded devices with threshold fluences on the order of ~200 µJ/cm^2.

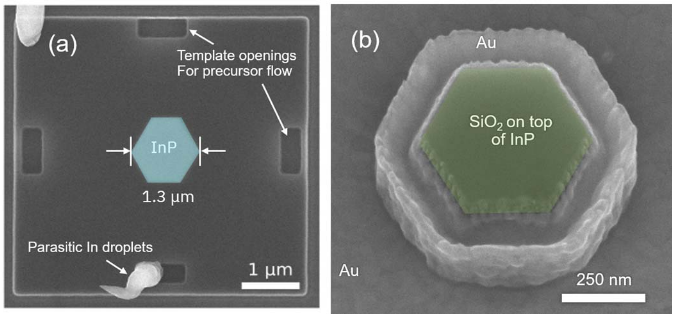

Figure 2 False coloured SEM images showing examples of (a) directly TASE grown InP microdisk inside the template and (b) gold cladded micro-cavity laser based on wafer bonding of InP.

In [8] a study of the scaling laws of plasmonic lasers was presented. Furthermore, metal-clad cavities, also referred to as hybrid plasmonic-photonic cavities, are explored to further scale the InP cavities beyond the diffraction limit. We simulate, design InP whispering gallery mode cavities with resonances in the near infrared (NIR) and fabricate these using the direct wafer bonding method. Whispering gallery mode cavities are dry etched into InP bonded on Si with diameters ranging from 100 nm to 1000 nm. In a second step some cavities are cladded with Au and we compare performance of purely photonic and hybrid plasmonic-photonic devices, in particular with focus on the geometrical scaling. 3D simulations with Lumerical FDTD solutions are used to analyze lasing behavior in the two cases.

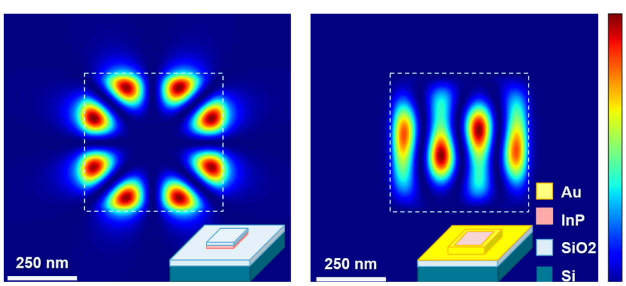

Figure 3 Example of optical mode simulation using Lumerical FDTD solutions for a 500 nm wide InP square cavity without Au (left) and with (right) Au. The top view of the mode is taken in the middle of the InP region the dashed lines show the borders of the InP.

Using thermal simulations, we are investigating the temperature profile in nanolasers. When using Au-clad cavities the temperature inside the device is around an order of magnitude lower than for the purely dielectric case, which might also partly explain the improved lasing performance in small cavities.

Whereas, our devices so far have been based on optical pumping we are working on new generation of devices with electro-optical functionality. In [9] we have demonstrated monolithically integrated high-speed InGaAs detectors via TASE, operating at 32 GHz. These devices serve as a first step towards electrically actuated optical emission. Simulations using the Sentaurus software is being used to evaluate device performance and further explore the design space [10].

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