All-optical AND Logic Gate Based on Semiconductor Optical Amplifiers for Implementing Deep Recurrent Neural Networks

Badrul Alam, Andrea Ceschini, Antonello Rosato, Massimo Panella and Rita Asquini
Department of Information Engineering, Electronics and Telecommunications
University of Rome "La Sapienza", 00184 Rome, Italy
e-mail: rita.asquini@uniroma1.it

***Abstract*— The development of optical logic gates is a key factor for enabling next generation of computations in the context of Deep Learning and Quantum Computing. In this work, we introduce a scheme for the implementation of an all-optical AND logic gate, which makes use of semiconductor optical amplifiers (SOA) in cross-phase modulation configuration combined with an all-optical XOR gate. Our analysis includes a realistic model of SOA, which considers also the phase and the delay of the signals. We prove that our scheme allows us to obtain almost ideal transitions in 3 out of the 4 situations in a 2-bit logic, with any SOA. The remaining combination shows a reduction of extinction ratio, which can still be improved with better tuning of SOAs.**

Keywords—all-optical logic gate, cross phase modulation, Semiconductor Optical Amplifier, recurrent neural network.

I. Introduction

In Deep Learning, dynamical layers as Long Short-Term Memory (LSTM) and Gated Recurrent Unit (GRU) enable the use of recurrent neural network architectures that include also feedback connections in addition to feedforward data processing [1]. Those networks are suited to classification, regression and prediction of time series data, in real problems such as speech/handwriting recognition, fast routing of optical networks, smart grids, and so forth. When dealing with the hardware implementation of such models, it is mandatory to rely on finite precision arithmetic and on the approximation of the gating mechanism, both in LSTM and GRU layers, by using Boolean logic [2].

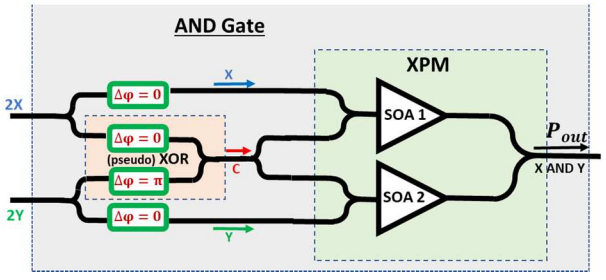

Fig. 1. Scheme of the all-optical AND logic gate composed by a XOR gate and an XPM configuration.

In this context, we introduce herein the scheme of an all-optical AND logic gate and we numerically analyze the evolution of the signal. This circuit, represented in Fig. 1, is composed of multiple basic optical passive elements, such as splitters/couplers and phase shifters, and also more complex active elements, such as semiconductor optical amplifiers (SOAs) in cross-phase modulation (XPM) configuration. A key role is given to SOAs in their high gain region, which required the development of specific numerical models. The signal considered in our study is transitioned with non-ideal filters and it is similar to existing NRZ data streams in real systems [3]. The scheme presented in this work fits the implementation through optical fiber technology or also other optical integrated platforms [4-7].

II. Optical Configuration and Simulation Settings

In the present analysis, the circuit considers a single mode propagating through guided wave platforms. The optical signals are streams of 10 Gbit/s (period 0.1 ns) NRZ modulated signals, with carrier wavelength λ_0=1550 nm and input power at 1 mW (0 dBm). To be closer to experimental situations, we have introduced a white noise (SNR=22 dB) and a distortion of the signal due to phase noise of the carrier and non-ideal filtering.

The simulations have been operated through Simulink™, by using suited scripting functions for the optical elements. The elements involved in the scheme are mainly standard coupler/splitters and phase shifters, whose operation have been considered ideal. In addition, in the XPM section two identical SOAs are set in parallel. The numerical model of the amplifiers has been obtained through a combination between the parameters available in the literature [8, 9] and in the device's datasheet (i.e., Thorlabs™ BOA1007H).

TABLE I
Parameters of the Adopted SOA

Characteristic	Value
Saturation power	18 dB
Unsaturated gain	30 dB @ 600 mA
Gamma factor	0.3
Cross-section area	$6{\cdot}2{\cdot}10^{-13}$ m^2
Alpha factor (α)	5
Length (L)	1500 μm
Effective Index (n_{eff})	3.390
Wavelength (λ)	1.55 μm

Phase shift was approximated with the formula:

$$\varphi = \frac{2\pi}{\lambda} \cdot n_{\text{eff}} \cdot L + \alpha\big(\ln(G) - \ln(G_0)\big), \qquad (1)$$

where symbols are listed in Table I. The second term in (1) indicates the shift $\Delta\varphi$ dependent on the optical signal itself. The comparison between the SOA model and experimental data is shown in Fig. 2(a). The amplitude gain and phase shifts in the SOAs are shown in Figs. 2(b) and 2(c), respectively, in relation with the amplitude of the input optical signal and with different values of the saturation power, which depend on the feeding current.

III. Analysis and Description

As it can be seen from the schematic view in Fig. 1, the circuit is divided into three main stages. In the first stage, the signals in X and Y lines, both with amplitude value 2S, are split into two branches; half of X and Y reach a "pseudo"

978-1-6654-7899-1/22/$31.00 ©2022 IEEE

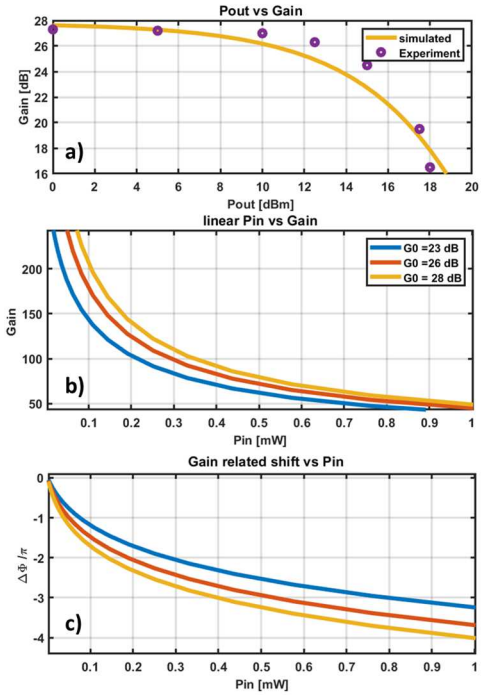

Fig. 2. Cladding refractive index vs. twist angle.

XOR gate, where one of the two branches is phase shifted by π radians. At the end of this stage, the two signals combine and constructive/destructive interference produce a new signal, which is referred to as C. In order to guarantee the synchronization, 'off-state' phase shifters of the same model are attached on the other parallel signal lines. In Table II, the truth table is shown where 'C' indicates the output of the XOR, and 'X', 'Y' are the logic values associated with the top and bottom lines.

TABLE II
TRUTH TABLE, WHERE S IS THE SIGNAL AMPLITUDE AND A IS THE SOA'S AMPLIFICATION IN PRESENCE OF S.

In	X	C	Y	X AND Y
00	0	0	0	0
01	0	$S \cdot e^{i\pi}$	S	0
10	S	S	0	0*
11	S	0	S	2·A·S

Before reaching the XPM stage, the signal in C is split into two halves, which are combined with X and Y. Depending on the phases of the two signal lines, the result of the combination may feature constructive and destructive interferences. In '00', the output is 0 excluding white noise. In '01', the signal in the two branches has S/2 amplitude and mutual phase shift of π. In '11', both SOAs have inputs at amplitude S and in phase and hence, the resulting constructive interference yields 2·A·S. The situation in '10' requires a careful approach; here, the top SOA has input 1.5·S and bottom SOA has input 0.5·S, both in phase. At the recombination stage of the SOA outputs, we would have:

$$P_{\text{out}} = \frac{1}{2} A_{\frac{S}{2}} \cdot \exp(i\Delta\varphi_{\frac{S}{2}}) + \frac{3}{2} A_{\frac{3S}{2}} \cdot \exp(i\Delta\varphi_{\frac{3S}{2}}), \qquad (2)$$

where we require to have P_{out} equal to 0. To this end, we set S at 0.5 mW to have a phase shift π between 0.25 mW and 0.75 mW and also to have close values of amplitudes. The results in the overall simulation are shown in Fig. 3; the system responds perfectly for the three combinations '00', '01', '11', while in '10' the output is non-ideal, although still with a significant extinction ratio.

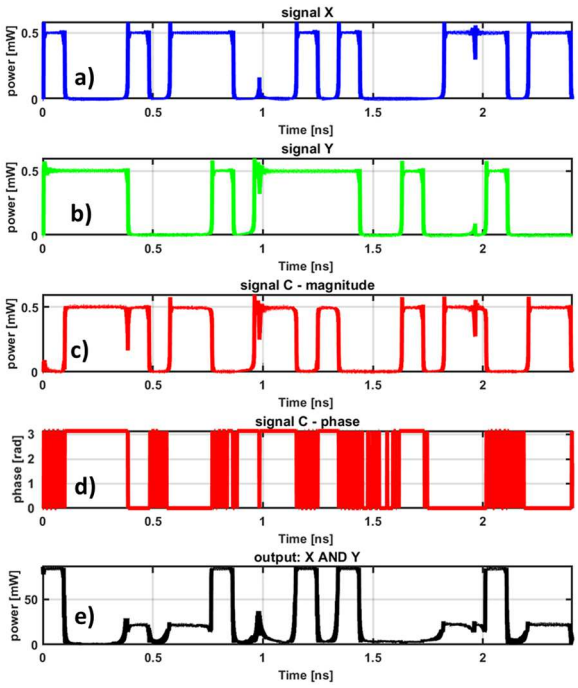

Fig. 3. Characteristics of the signals: X amplitude (a); Y amplitude (b); C amplitude (c); C phase (d); output amplitude of the device (e).

IV. CONCLUSIONS

Our analysis on the presented all-optical AND logic gate shows encouraging results. The combinations '00', '01' and '11' work with quasi-ideal performance and they can be implemented with any setting from the SOAs. The accuracy of the '10' combination is more challenging, but specific adjustments in the single amplifier can guarantee a reasonably small extinction ratio. We have also indicated the key conditions for an ideal resolution of the '10' solution, which is related to the design of SOAs. While present amplifiers are developed for applications in telecommunication systems, future devices can be designed to satisfy the requirements even for all-optical deep recurrent neural networks, as we proved that the development of such all-optical logic gates is possible.

REFERENCES

[1] Y. Yu, et al., "A Review of Recurrent Neural Networks: LSTM Cells and Network Architectures", *Neural Comput.*, vol. 31, pp. 1235-1270, 2019.

[2] A. Ceschini, A. Rosato, and M. Panella, "Design of an LSTM Cell on a Quantum Hardware", *IEEE Trans. Circuits Syst. II - Express Briefs*, vol. 69, no. 3, pp. 1822-1826, 2022.

[3] R. Ramaswami et al., *Optical Networks, A Practical Perspective*, third edition, Elsevier, ch. 3.3, pp. 121-171, 2010.

[4] W. Bogaerts, et al., "Programmable photonic circuits", *Nature*, vol. 586, pp. 207-216, 2020.

[5] B. Alam, et al., "Numerical and Experimental Analysis of On-Chip Optical Wireless Links in Presence of Obstacles", *IEEE Photonics Journal*, vol. 13, no. 1, pp. 1-11, 2021.

[6] R. Asquini, et al. "Integrated evanescent waveguide detector for optical sensing", *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 8, no. 7, pp. 1180-1186, 2018.

[7] A. Buzzin, et al., "Evanescent Waveguide Lab-on-Chip for Optical Biosensing in Food Quality Control", *Photonics Research,* vol. 10, no. 6, pp. 1453-1461, 2022.

[8] M.J. Connelly, *Semiconductor Optical Amplifiers.* Chapter 3, Springer, 2002.

[9] A. Kapoor, et al., "Saturation characteristics of InGaAsP-InP bulk SOA", *Proc. SPIE*, 7597, Physics and Simulation of Optoelectronic Devices XVIII, 75971I, 2010.