Physical Layer Modelling of Semiconductor Optical Amplifier Based Terabit/second Switch Fabrics

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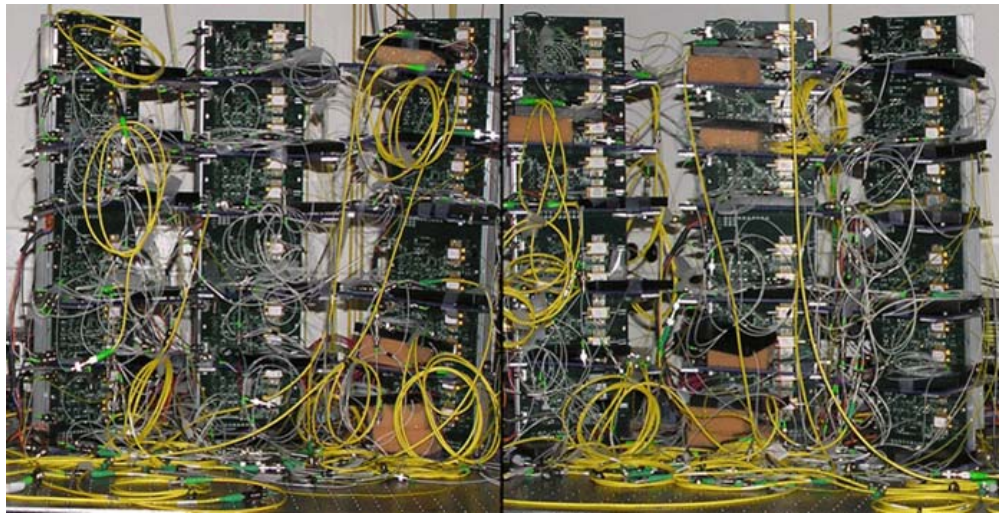
Where innovation starts

Outline

- **Motivation for studying semiconductor optical amplifier switch fabrics**
  - Low latency reconfigurable interconnects in high performance computing
  - Emerging scalable photonic integrated switch circuits
  - Viability of multistage switch architectures for large scale interconnection
- **Simulator architecture**
  - Multiwavelength emulator
  - Power penalty estimation
  - Performance mapping for multi-stage networks
- **Switch fabric performance**
  - Calibration
  - Scaling capacity - multi-wavelength operation
  - Scaling connectivity - input power dynamic range
- **Conclusions**

Low latency reconfigurable interconnects



Terabit/second SOA based 12x12 Data Vortex Shacham JLT, 23, (10), 3066-3075, (Oct 2005).

- High performance computing, future server networks, requiring Terabit/second low latency interconnection with several tens of high bandwidth ports
- Sophisticated testbeds devised and implemented increasing numbers of groups
- Colourless SOA switches promising for routing of high capacity WDM packets. Good crosstalk, ease of use and integration being key.
- HOWEVER: Concerns over accumulating noise and distortion

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Emerging integrated switch technology

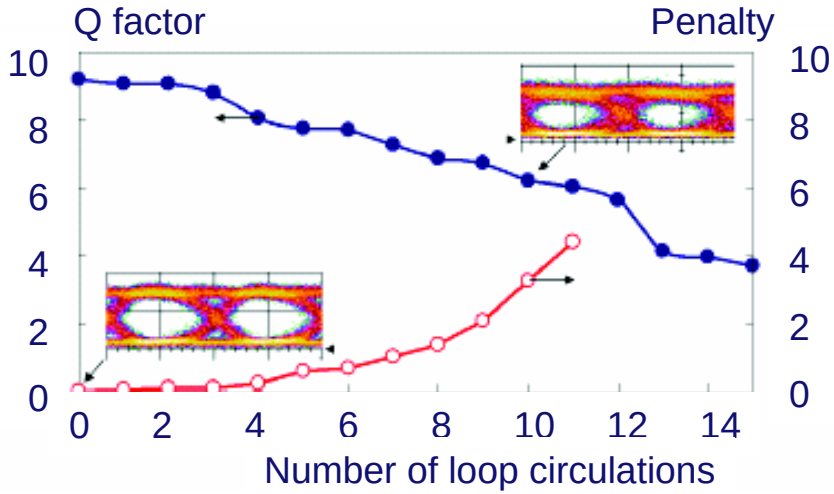
• Highly cascadability demonstrated for quantum dot based switches
Liu, CLEO 2006

• Uncooled power efficient (70ºC) 2x2 QD switches demonstrated
Aw, CLEO 2008

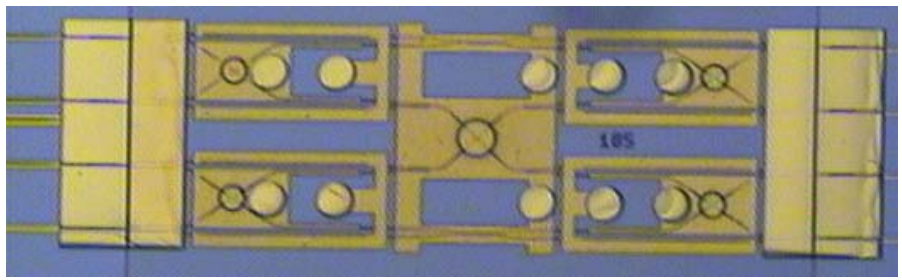
• Low power penalty routing demonstrated with 4 input 4 output multi-stage switch circuits
Albores-Mejia, Photonics in Switching 2008

• Larger monolithic switch matrices now becoming tractable

BUT little study into the scaling limits for broadband SOA based switches

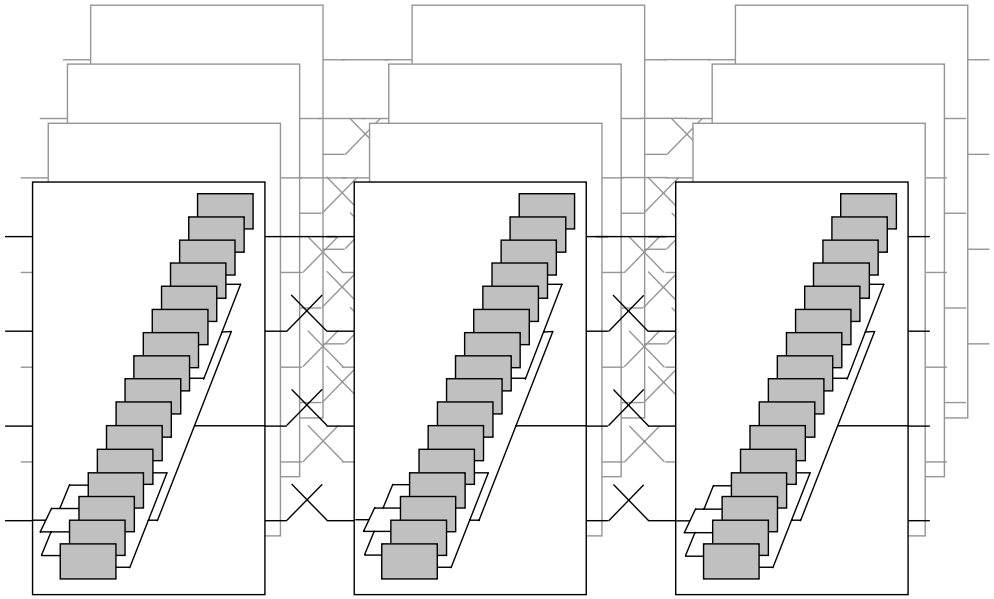


Discrete cascaded QD SOAs

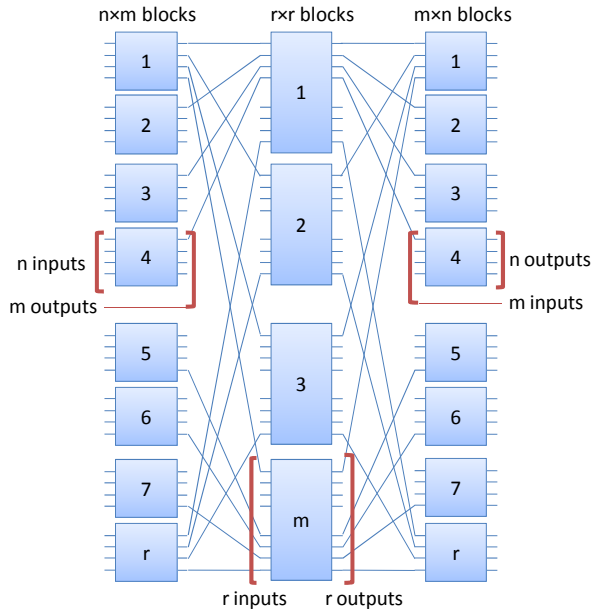


Integrated multistage circuits

Multi-stage switch fabrics: Clos networks



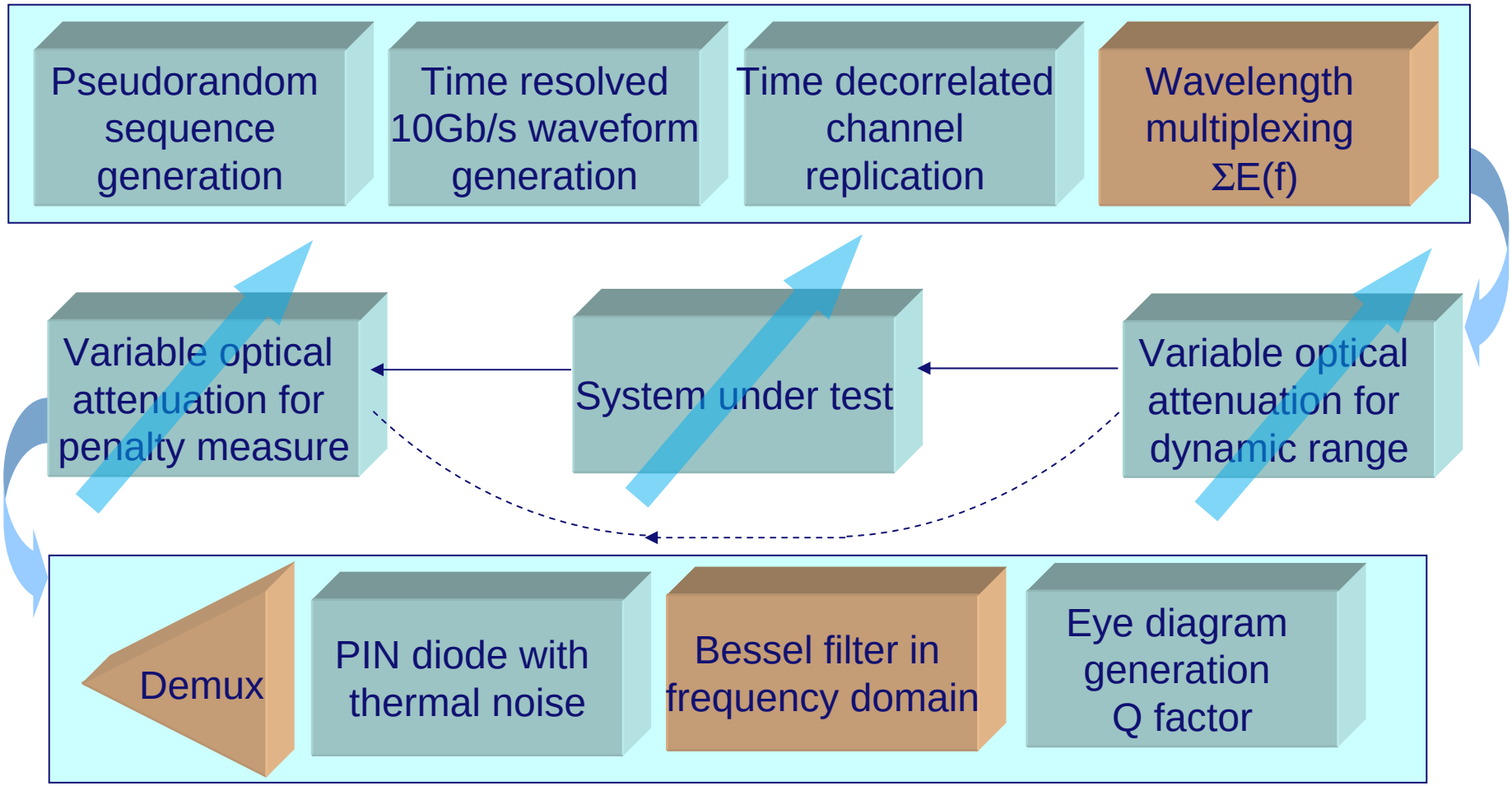
16x16



Generalised three stage

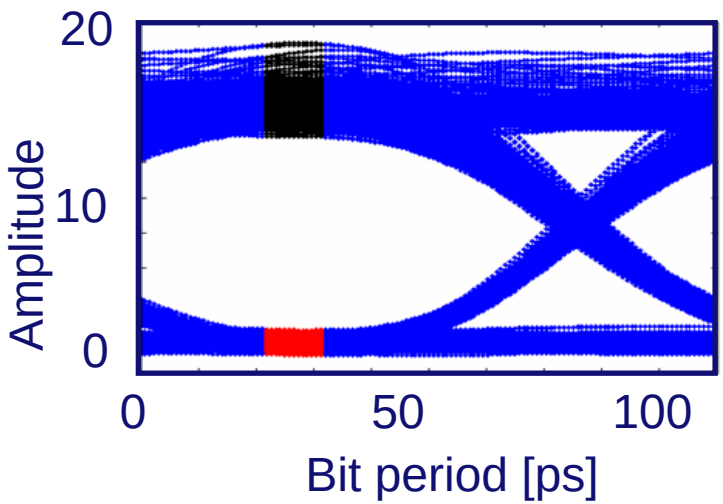
- Clos networks offer good compromise between number of stages (power consumption, power penalty) and connection scaling
- Scaling assessed by studying the data integrity at the physical layer for varied data capacity per port for three stage networks
- Large networks feasible by introducing increasing numbers of splitters at each stage

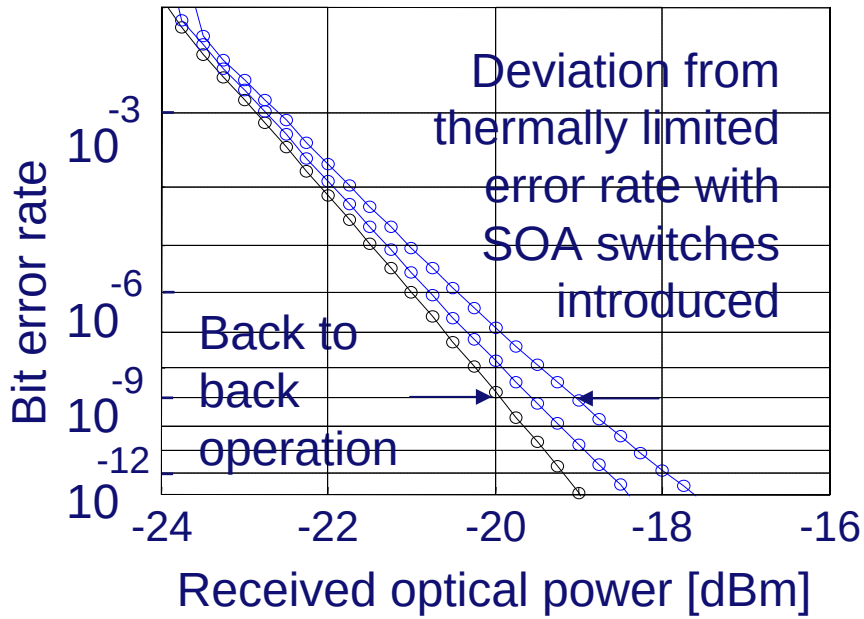
Wavelength multiplexed link simulation



- Mixed time and frequency domain units cascaded for power penalty evaluation from Q factor

Power penalty evaluation

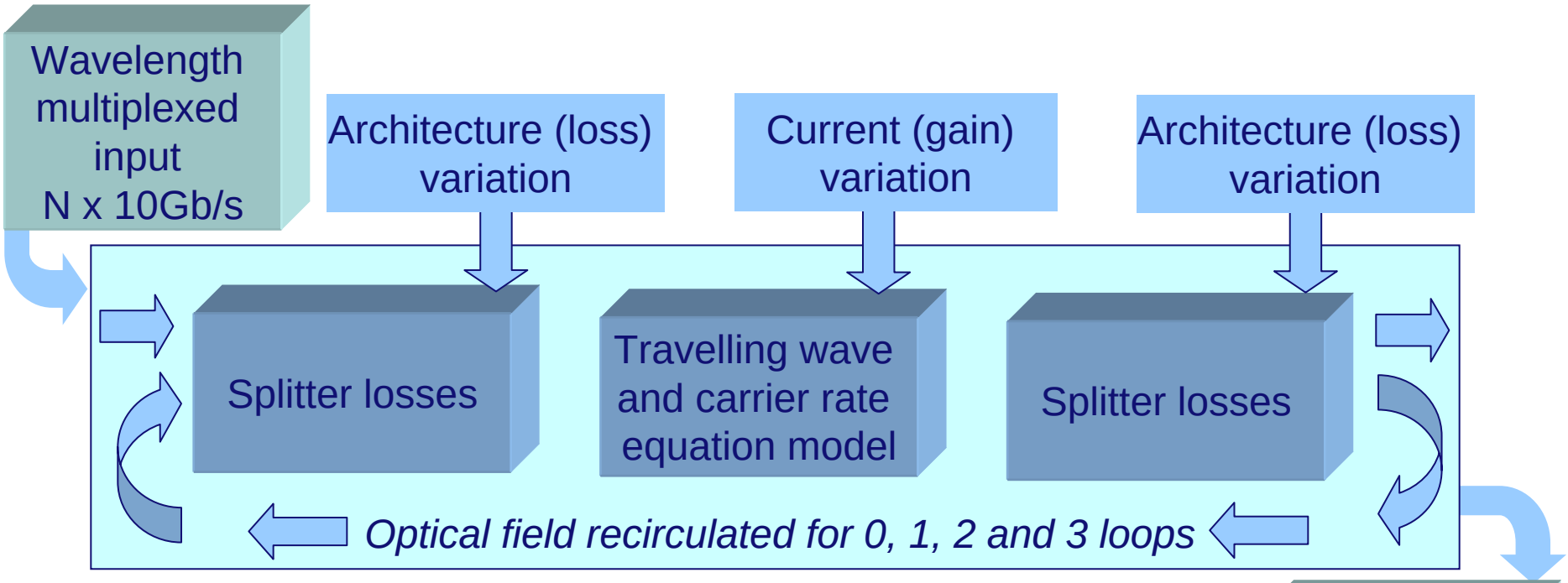




- Time resolved receiver output time-wrapped to generate eye diagram
- Centre of eye opening windowed by locating level transitions
- Probability density functions generated from ones (black) and zeros (red)
- Bit error rates correlate with Q factors for Gaussian PDFs
- Specify power penalty at BER=10^{-9}

E. Desurvire, Erbium doped fiber amplifiers, Wiley

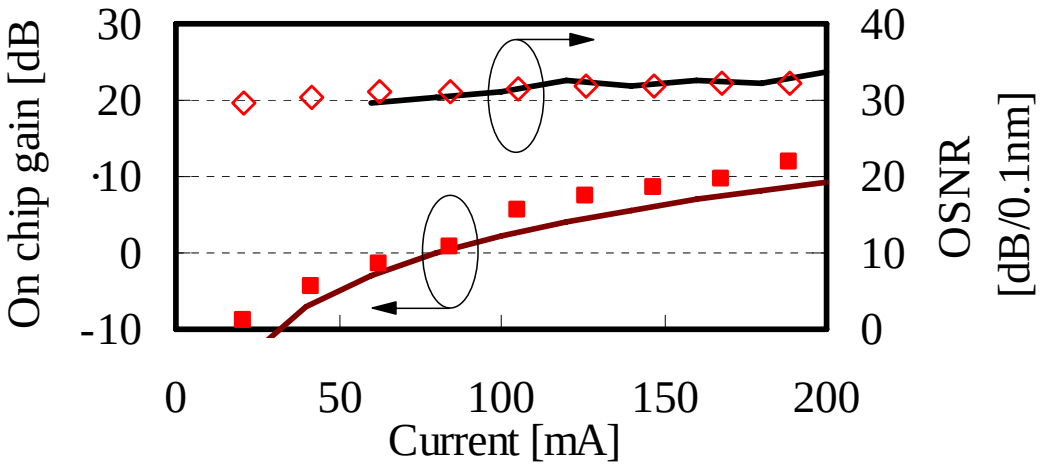
Switch fabric definition

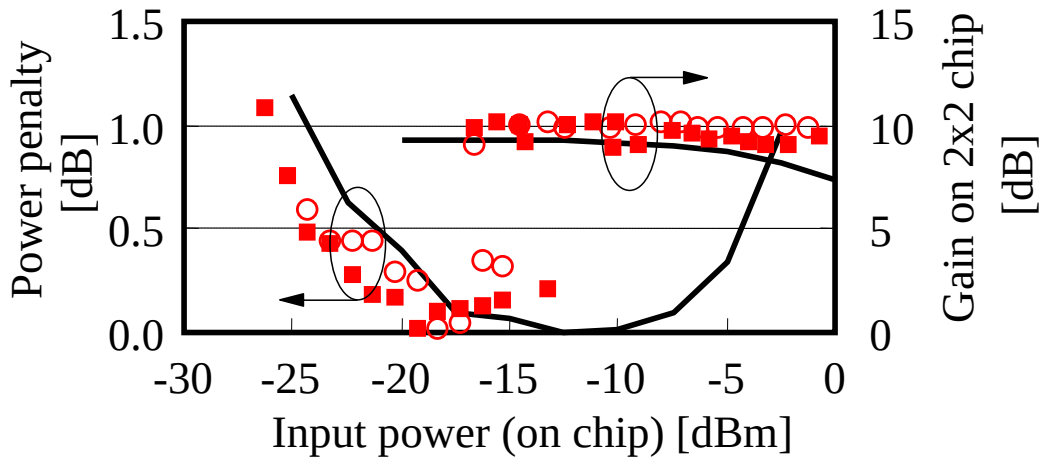


- Splitter losses scanned to study range of connection configurations
- Currents scanned to identify local optima
- Input power scanned at system input

Travelling wave algorithm as per
Distributed Feedback Semiconductor Lasers
Carroll, Whiteaway, Plumb, IEE, 1998

Travelling wave model calibration

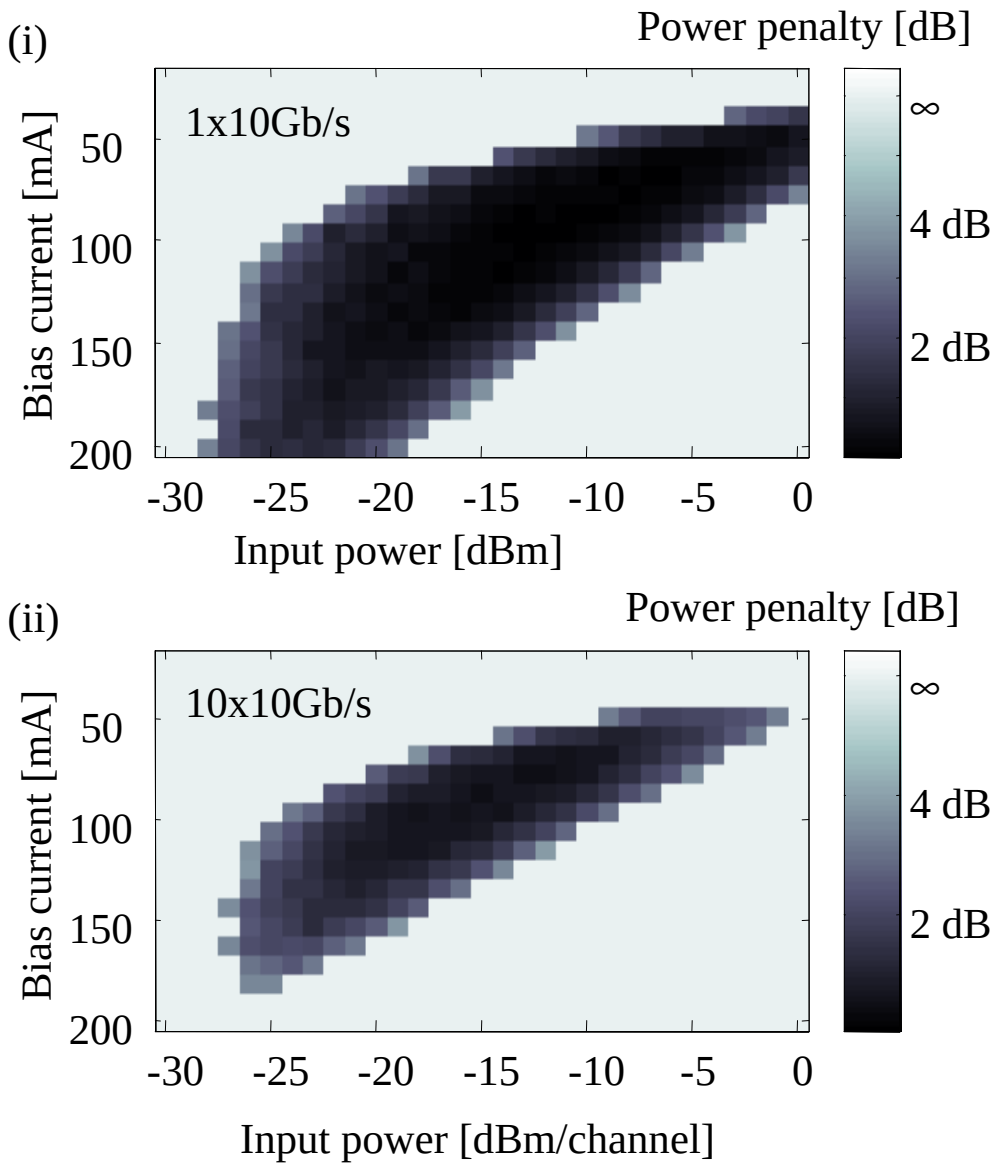




- Calibration of model for performance of uncooled 2x2 switch circuits
- Benchmarked as a function of input current and input power
- Logarithmic gain carrier relationship. No wavelength dependence implemented.

Experimental data from Aw, CLEO 2008

Power penalty performance



- Data shown for three stage 16x16 switch implemented with 4x4 stages
- Extensive operating range for single wavelength operation
- Distortion evident at high input power and high current
- Distortion threshold further reduced through increased aggregate power
- Optimum current conditions selected for broader architecture comparisons

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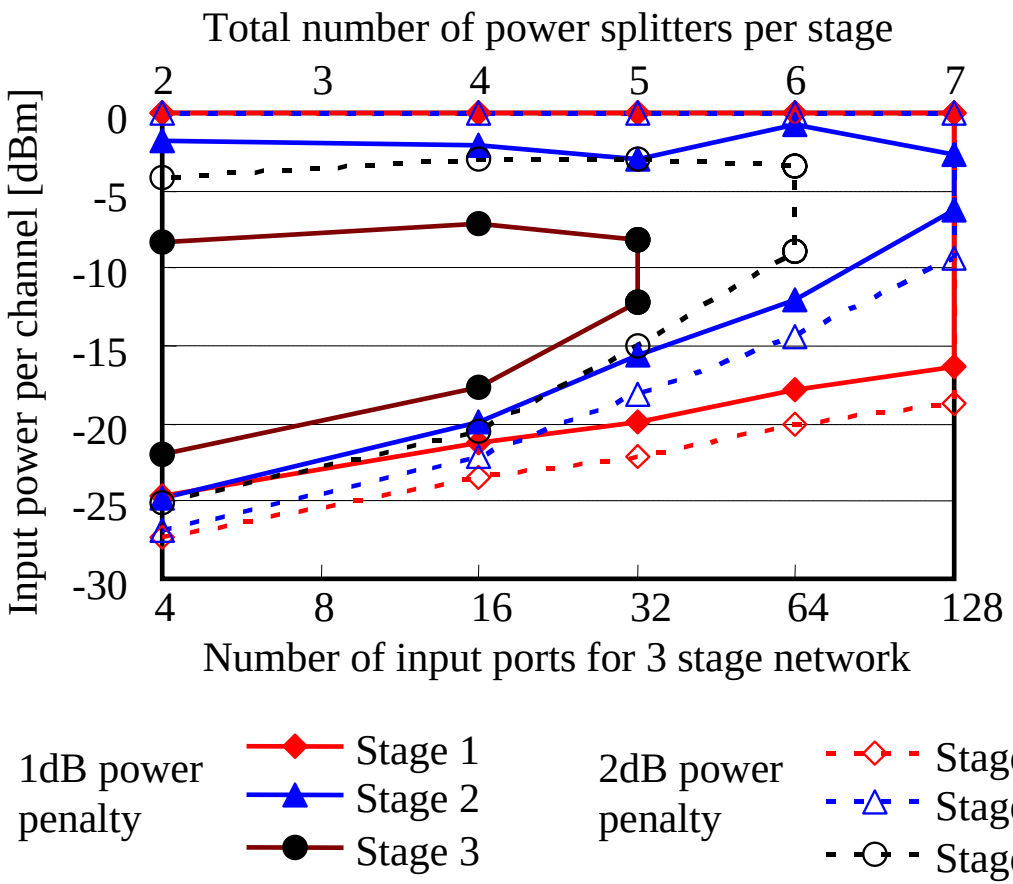
Multi-stage input power dynamic range



- Multiple simulations for broader range of power maps enables comparison of connection levels
- Dynamic range reduced at each consecutive stage
- Distortion limited at high power
- Noise limited at low power
- The combined effect ultimately limits feasible power maps and connectivity
- 1dB power penalty for 32x32
- 2dB power penalty for 64x64

Conclusions

- Three stage switch fabrics analysed for Clos switching networks with SOAs
  - Low penalty multiwavelength routing of 10x10Gb/s payloads shown
- High data capacity feasible in large scale switch fabrics
  - 32x32 switch fabric feasible with 1dB power penalty
  - 64x64 switch fabric indicates 2dB power penalty
  - Further scaling conceivable with further active element optimisation
- Competive system level figures of merit
  - <1W per 100Gb/s path indicating <10mW/Gb/s driver power efficiency
  - Extrapolated 6.4Tb/s aggregate capacity for 64 ports at 10x10Gb/s
  - Encouraging for next generation integrated switch technologies

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